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MEASUREMENT OF TRANSIT TIME AND RELATED TRANSISTOR CHARACTERISTICS

D. E. Sawyer and G. J. Rogers
National Bureau of Standards
Washington, DC 20234

and

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National Bureau of Standards
Boulder, CO 80302

TECHNICAL REPORT NO. AFWL-TR-73-54

October 1973

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FOREWORD

This report was prepared by the National Bureau of Standards, Institute for Applied Technology, Washington, DC, and National Bureau of Standards, Institute for Basic Standards, Boulder Colorado, under Contract F29601-71-F-0002. The research was performed under Program Element 62601F, Project 8809, Task 11.

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This technical report has been reviewed and is approved.

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ABSTRACT

Two instruments for transistor delay-time measurements, the vector voltmeter and Sandia bridge, were analyzed and comparative measurements were made on several types of commercial and two special transistors. It was found that extraneous pickup at the measurement frequency can cause large errors in measured delay time. A technique for minimizing these errors was developed and verified for the Sandia bridge by removing the frequency dependence of delay times measured on tiny plug-in R-C networks. Measurements of probe restoring force, probe tip protrusion and lateral motion (skating) with loading were recorded for special probe assemblies to be used in an automatic wafer prober for measurements on transistors in custom-designed integrated circuit wafers. The data is used to assist in adjusting the probers. A technique was developed for determining the effects of the probe assemblies on transistor measurements made from 0.1 to 2.0 GHz. Each probe assembly may be represented by an equivalent circuit consisting of three unknowns; these unknowns are determined by making impedance measurements at the input connectors with the probe tips contacted by combinations of open circuits, short circuits, and resistors of known value. Arrays of such terminations were successfully fabricated and characterized. An S-parameter interlaboratory testing program was developed. The plan calls for six of each of three types of transistors to be measured by participants at frequencies from 0.11 to 2.0 GHz. Additionally, a 10-dB attenuator and R-C networks on TO-72 headers are to be circulated to pinpoint measurement discrepancies.

This printing is identical with the original printing except for typographical corrections made on pages 13 and 110 and removal of the distribution limitation. Unlimited distribution was authorized by the Air Force 23 October 1973.

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SECTION I

INTRODUCTION

In response to a request from the Air Force Weapons Laboratory (AFWL), the National Bureau of Standards (NBS) undertook a three-part project to assist in improving instrumentation and procedures utilized in measurements associated with the prediction of the effects of nuclear radiation on semiconductor devices. The topics to be treated were the resolution of some causes of transistor transit-time measurement discrepancy, the development of techniques to facilitate high-frequency measurements on transistors in an IC wafer, and the development of an interlaboratory test of transistor S-parameter measurement procedures. This report covers the work on these topics accomplished during the period January 27, 1971 through August 31, 1972. The work was performed by D.E. Sawyer, G.J. Rogers, F.H. Brewer, T.F. Leedy, K.O. Leedy, and P.M. Sandow of the Electronic Technology Division, Institute of Applied Technology, Washington, D.C., and L.E. Huntley of the Electromagnetics Division, Institute for Basic Standards, Boulder, Co.

1. TRANSIT TIME MEASUREMENTS

One cause of failure of semiconductor devices in a radiation environment is reduction of minority carrier lifetime as a result of irradiation by neutrons. In the case of bipolar transistors, this reduction is manifested by a loss of gain of the device. However, difficulties exist in measurements characterizing devices as attested by widespread differences in results. With regard to bipolar transistors, the so-called base transit time is a parameter which has appeared to correlate with the resistance of the device to degradation by neutron irradiation. However, investigations made prior to the present study have shown that it may be difficult to achieve the required measurement precision when measurements are made on the same device

at various test facilities using the same type of apparatus, or even at the same laboratory with different apparatus. This raised serious questions as to the reliability of base transit time as a predictor of device degradation.

The resolution of some of the causes of transit time measurement discrepancy is reported in Section II. The section begins with an operational definition of delay time and proceeds through the analysis of two instruments, one based on a vector voltmeter (reference 1) and the other a Sandia bridge (reference 2). Explicit expressions were obtained for the dependence of the measured delay time on the passive elements of the transistor as well as on the parameters representing active processes such as carrier drift and diffusion across the base. A fairly simple technique was developed to calibrate the vector voltmeter itself. Tiny R-C plug-in networks of known delay time were designed and fabricated for use in calibrating and checking delay-time instruments. Extraneous coupling at the measurement frequency was discovered to be a significant possible cause of discrepancies in measured values of delay time. A technique which should be generally useful for all phase delay-time measurement systems was developed to obtain the magnitude and location of such error-producing sources within the measurement circuit. With the sources so specified, it is a straightforward matter to correct for their influence on measurements on transistors or other networks of known configuration. The error-correcting technique was demonstrated using a version of the Sandia bridge constructed at NBS. Finally, intralaboratory and interlaboratory transistor delay time measurements are presented to show the variations that are representative if corrections for the effects of the measurement circuits are not made.

2. HIGH FREQUENCY PROBE MEASUREMENTS

Characterizing parameters, such as delay time, of individual transistors of an integrated circuit (IC) before the IC elements are interconnected is under investigation at the AFWL in the expectation that this will offer an effective means for hardness assurance and quality-control

screening. Since final packaging usually is the most expensive step in device manufacturing, weeding out unsatisfactory transistors at an early stage may also have an economic benefit. One technique for characterizing devices at the wafer level is to use probes to contact the transistor electrodes. Implementing such measurements, particularly at frequencies in the range of hundreds of megahertz to several gigahertz, the range within which transistor cut-off frequencies for today's devices lie, in conjunction with modern measurement apparatus, such as automatic probers and computer-controlled analyzers, raises a number of questions which must be answered before one can have confidence in the outcome. The questions range from those of a mechanical nature, such as a recognized need for data which would allow the prober to be adjusted to ensure reliable contact between the probe tips and the transistor contact pads, through questions of a hybrid mechanical-electrical nature, such as the effect of probe pressure on intrinsic device parameters, to questions more completely electrical, such as the effects of the electrical nature of the probe assembly itself on transistor data obtained through use of the probes. Section III treats these questions and presents reasons why contact pressure should not be applied to active device regions and a technique for determing the network values in an equivalent network representation of the probe assembly.

3. S-PARAMETER MEASUREMENTS

One may determine delay times and other quantities useful for predicting radiation hardness (such as f_T, the frequency at which the common-emitter current gain is unity) from scattering parameter, or S-parameter, measurements. These techniques offer a number of advantages for small-signal, high-frequency transistor measurements, and their use is becoming more popular for characterizing devices. The NBS designed a transistor S-parameter interlaboratory round-robin test for AFWL with the purpose of helping AFWL assess the uniformity of these measurements among various laboratories and manufacturing facilities. The round robin is designed to reveal the causes of measurement discrepancies, if descrepancies arise. To facilitate

this objective, the round-robin plan, described in Section IV, includes among the items to be circulated several passive networks in addition to the transistors themselves. Measurements are to be made on all the items at frequencies from 0.11 to 2.0 GHz. Six each of three types of transistors selected as representative of those designed to satisfy three different circuit requirements are to be measured with emitter currents between 1.6 and 10 ma.

SECTION II

TRANSISTOR DELAY TIME

1. OPERATIONAL DEFINITION AND EXAMPLES

The transfer function $H(\omega)$ of an electrical component, or electrical system, is the ratio of output to input current or voltage, specified as a function of the input frequency ω, and may be written

$$H(\omega) = A(\omega)e^{-j\Theta(\omega)}. \tag{1}$$

For physically real components or systems, $A(\omega)$ is pure real and is an even function, and $\theta(\omega)$ is odd. The phase delay time, τ_{ph}, and the group delay time, τ_{gr}, are (reference 3):

$$\tau_{ph} = \frac{\theta(\omega)}{\omega} \tag{2a}$$

and

$$\tau_{gr} = \frac{d\theta(\omega)}{d\omega}. \tag{2b}$$

The phase delay time is the delay time associated with the phase shift of the carrier frequency ω. The group delay time is the delay time of the envelope of the input signal and represents the propagation delay of the information contained in the input signal.

a. Delay Time of Lossless, Nondispersive Transmission Lines. The quantity $A(\omega)$ for a lossless, nondispersive transmission line is unity and the phase angle $\theta(\omega)$ is $\omega\tau$, where τ is proportional to the length of the line and is fixed if the line length is fixed. Thus,

$$H(\omega) = e^{-j\omega\tau} \tag{3}$$

and, from equation 2, the phase and group delay times are the same:

$$\tau_{ph} = \tau_{gr} = \tau \qquad (4)$$

Equation 4 suggests that calibrated transmission lines of adjustable length can be used to introduce known values of delay times into circuits; this is the means used to achieve phase balance in the Sandia bridge described in Section II 2b.

b. Phase Delay of an R-C Network. Some instruments such as the vector voltmeter setup described in Section II 2a determine delay time by measuring the phase shift between the small-signal emitter and collector currents. Let us now consider the simple R-C circuit shown in figure 1a and imagine that it has been assembled on a transistor header: the terminals E, B, and C, respectively, represent the emitter, base, and collector header leads.

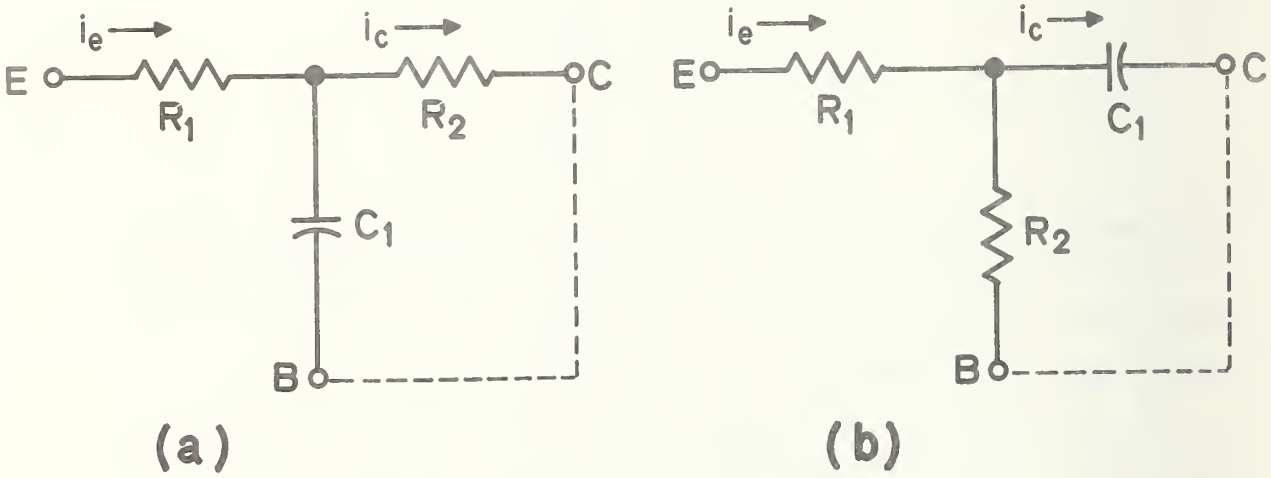

Figure 1. Plug-in R-C Delay Networks. The Components May Be Arranged to Yield Either Delay Time (a), or a Negative Phase Delay Time (b).

The line shown dotted between B and C represents an a-c short-circuit in the measurement circuit achieved through the use of a capacitor across the transistor socket. We readily find that the collector and emitter currents are related as

$$\frac{i_c}{i_e} = \frac{1-j\omega R_2 C_1}{1+(\omega R_2 C_1)^2} = \left[1 + (\omega R_2 C_1)^2\right]^{-1/2} e^{-j \tan^{-1} \omega R_2 C_1} \qquad (5)$$

where the quantities in equation 5 are defined in figure 1a. Comparing the extreme right hand side of the above equation with equation 1, we identify $[1 + (\omega R_2 C)^2]^{-1/2}$ as $A(\omega)$, and $\tan^{-1} \omega R_2 C$ as $\theta(\omega)$. From equations 2, the phase and group time delays are

$$\tau_{ph} = \frac{1}{\omega} \tan^{-1} \omega R_2 C_1 \text{ and } \tau_{gr} = R_2 C_1 \left[1 + (\omega R_2 C_1)^2\right]^{-1} \qquad (6)$$

respectively. For $\omega R_2 C \ll 1$, the phase and group delays are both nearly equal to the product $R_2 C_1$.

c. Negative Phase Delay in an R-C Network. If, on the transistor header discussed above, we connect the elements as shown in figure 1b, we now find $A(\omega) = \omega R_2 C_1 \left[1 + (\omega R_2 C_1)^2\right]^{-1/2}$, and $\theta(\omega) = -\tan^{-1} 1/\omega R_2 C_1$. For this case $\tau_{ph} = \frac{-1}{\omega} \tan^{-1} 1/\omega R_2 C_1$ and is negative, while $\tau_{gr} = R_2 C_1 [1 + (\omega R_2 C_1)^2]^{-1}$ is positive (as it must be) and identical to the group delay for the network in figure 1a.

d. Simulation of a Transistor with an R-C Network. Simple R-C networks on transistor headers with known values of phase and group delay time can be used to calibrate transistor delay time measurement instruments. The delay times are as given above; we recognize $A(\omega)$ as the absolute magnitude of the common-base current gain of our equivalent "transistor". In Sections II 2a and II 2b, the use of these networks for testing transistor delay time measurement systems is described.

2. ANALYSIS

The measurement circuits considered in this section have the common characteristic that the a-c signal voltage between the transistor collector and base terminals is zero when the delay time is measured. This is accomplished in the Sandia bridge with the use of a "bucking" or "nulling" signal from a phase splitter and electrical delay circuit, and more simply in the vector voltmeter setup by bypassing the transistor collector to the base in a grounded, common base circuit. Because of this common operating characteristic, it is appropriate that both be analyzed in the same manner, and we shall show that the resulting expressions for measured delay time are similar generically.

A surprising result of this analysis is that neither circuit measures the sum of the propagation delays between the emitter and collector leads. On the contrary, certain time constants may diminish the measured delay time. This is because the measurement yields the phase, rather than the group delay time. As we shall see, the product of the base resistance and collector capacitance yields a negative contribution to the phase delay time.

The results for the most commonly applicable conditions of transistor design and device measurements are presented here; the more general analytic results are recorded in Appendices so that the applicability of the simplified, approximate expressions for the delay-time contributions can be verified for any particular case.

For analysis, we assume the widely used transistor model shown in figure 2. Although the circuit shown represents mesa devices quite well, other types of transistors might require the addition of other passive elements, such as an additional capacitor between the top of the current generator and the base contact B (to represent the base-collector overlap diode capacitance in a planar device), or a resistor in series with the collector terminal C (to represent the collector series resistance). If additional elements are used, additional terms will appear in the expression for the delay time.

In the model the quantities C_e and C_c are the transition-region capacitances of the emitter-base and base-collector junctions, respectively. The resistor r_b represents the base resistance, and the small-signal resistor r_e represents the dynamic resistance of the (forward biased) emitter junction. For forward emitter currents much larger than the emitter-base diode saturation current,

$$r_e = \frac{kT}{qI_E} \tag{7}$$

where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge, and I_E is the d-c emitter current. At room temperature, $kT/q = 26$ mV and so $r_e = (26/I_E)$ ohms for I_E in milliamperes.

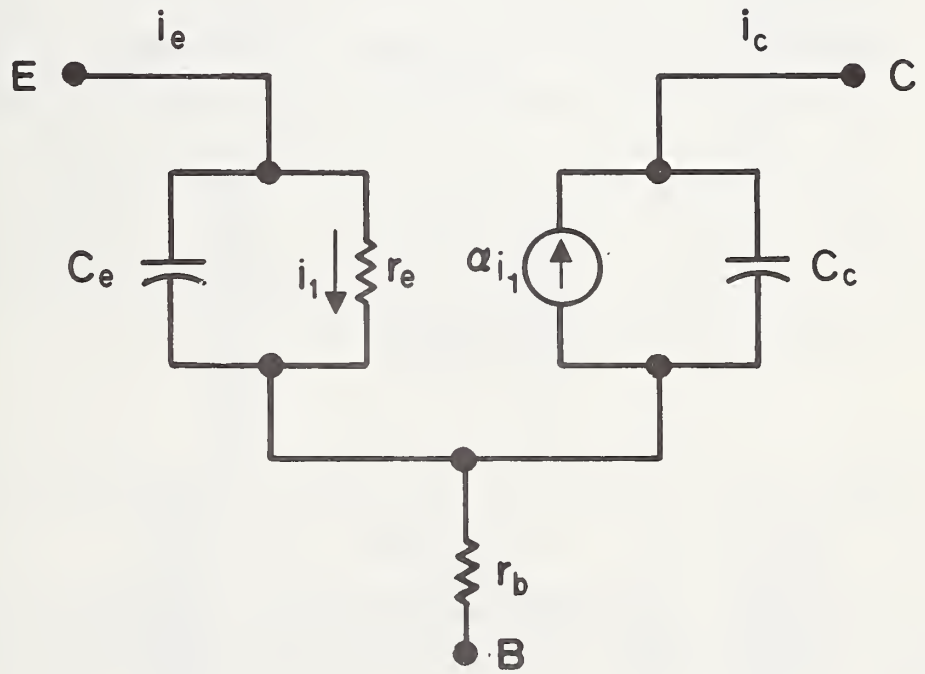

Figure 2. Transistor Model Used For The Analysis Of Delay Time Measurement Apparatus.

Only i_1, the current through r_e, is effective in producing transistor action. The current source in the collector circuit represents the active portion of the transistor operation and is specified as the product of i_1 and α, the small-signal base-transport coefficient. In general, α is complex and varies with frequency. It can always be written

$$\alpha = \alpha(\omega)e^{-j\omega\tau_\alpha} \tag{8}$$

where $\alpha(\omega)$ is an even function of frequency and τ_α is the delay time associated with the transit of minority carriers across the base region and collector junction. It is convenient to define the time constants $\tau_e \equiv r_e C_e$ and $\tau_{bc} \equiv r_b C_c$. We note from equation 7 that τ_e varies inversely with emitter current, and that it is negligibly small if sufficiently large emitter currents are used.

a. Vector Voltmeter. Figure 3 is a block diagram of the vector voltmeter delay time measurement apparatus. In this system, the vector voltmeter indicates the phase angle between signals applied to its A and B inputs. The signals for the inputs are obtained from current transformers in the transistor emitter and collector leads as shown in figure 4, the schematic diagram of the transistor test fixture. The transistor delay time is thus related to $\theta(\omega)$, the vector voltmeter phase angle, and may be found* with the use of equation 2a.

---

*For θ in degrees and the frequency, f, in hertz, the expression for τ in seconds is

$$\tau = \theta_{deg}/(360f)$$

A particularly useful form of this equation expresses the delay time in nanoseconds in terms of the frequency in megahertz and the phase angle in degrees:

$$\tau_{ns} = (2.777/f_{MHz}) \text{ per degree.}$$

A one degree phase shift at 27.77 MHz would indicate a delay time of 0.1 ns, for example.

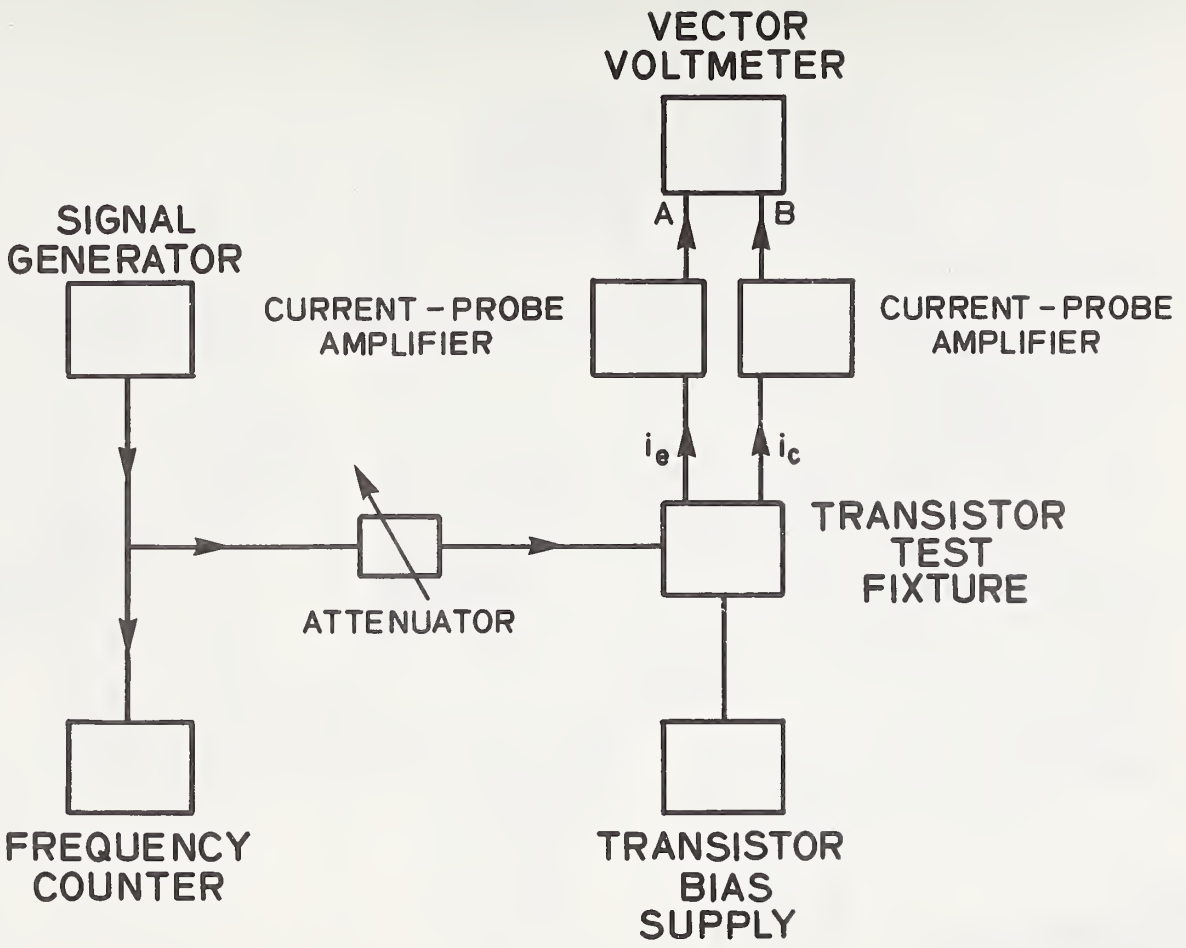

Figure 3. Block Diagram Of The Vector Voltmeter Delay Time Measurement Apparatus.

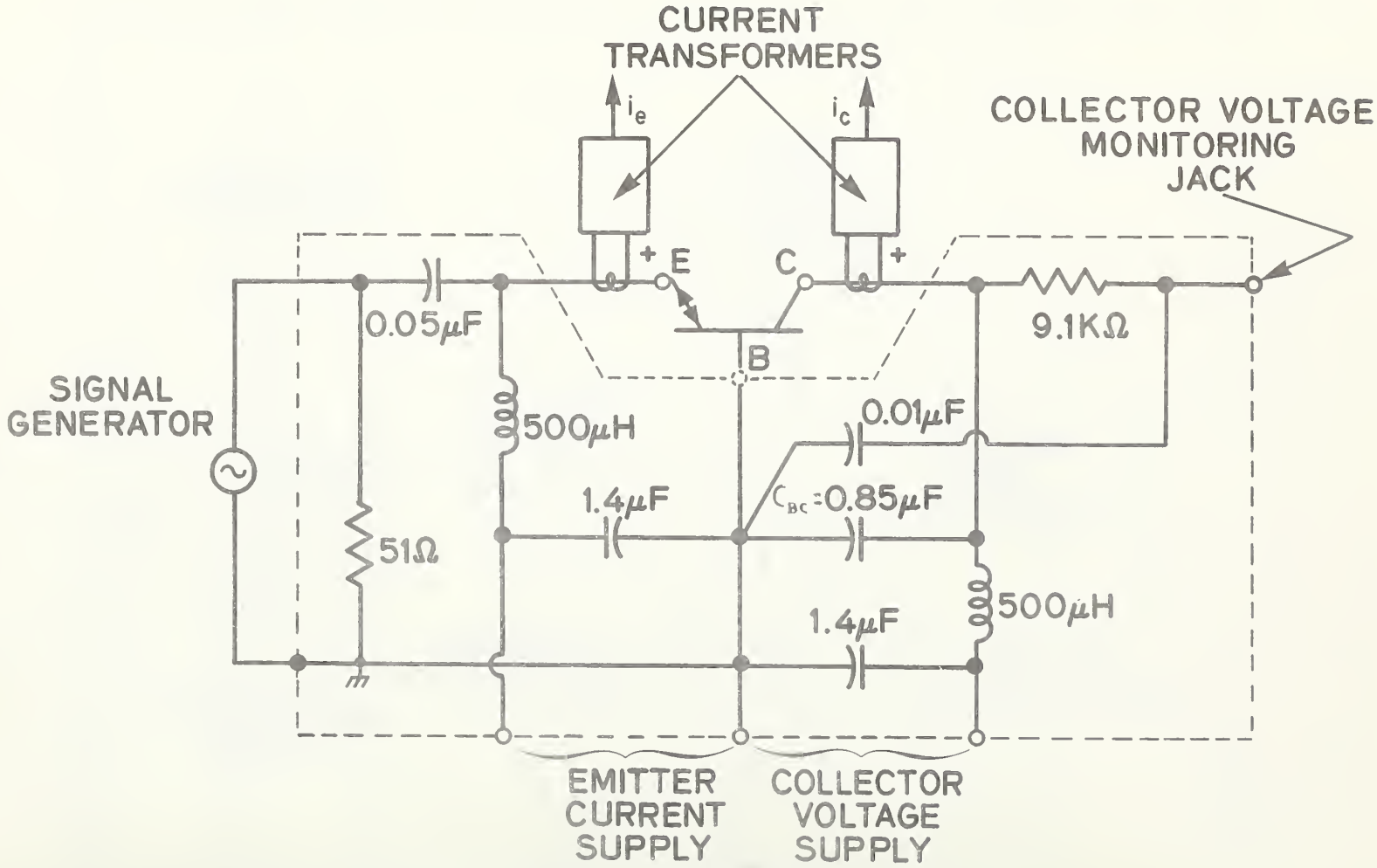

Figure 4. Transistor Test Fixture.

In Appendix I we show that τ, the delay time read from the vector voltmeter is related to the transit time τ_α and the time constants τ_e and τ_{bc} by

$$\tau = \tau_\alpha + \tau_e - \frac{\tau_{bc}}{h_{fe}} \tag{9}$$

where $h_{fe}=\alpha/(1-\alpha)$ is the small-signal common emitter current gain. We note that h_{fe}, rather than h_{fb}, appears in equation 9, even though the transistor base is the common element in the measurement circuit. Equation 9 quite accurately describes the idealized model shown in figure 2 providing that $\omega\tau << 1$, which is the usual state of affairs. If this condition is not fulfilled, then one must use the more general expression, equation 29 in Appendix I, to determine the delay time.

Equation 9 states that the delay time, as determined from the measured emitter-collector current phase angle, is the sum of τ_α and τ_e diminished by the collector-base R-C time constant divided by the common-emitter current gain. For most good-quality transistors h_{fe} is sufficiently large and τ_{bc} sufficiently small that the last term may be neglected, and the delay time measured is simply the sum of τ_α and τ_e. However, following irradiation, h_{fe} may drop and τ_{bc} increase via an increase in r_b; it is possible that the τ_{bc}/h_{fe} term may then affect the delay time measured.

b. Sandia Bridge. A detailed analysis of the Sandia bridge (reference 2) appears as Appendix II.

A circuit diagram of the bridge is shown in figure 5a and its equivalent circuit in figure 5b. The sources V_e and V_c are impressed signal sources and result from voltages induced by the signal generator in the emitter and collector coupling loops and phase shifted with variable-length emitter and collector lines. The sources V_a and V_b represent extraneous signal sources at the measurement frequency. The effects of V_a and V_b will be discussed in a following section; for the present it is assumed that V_a and V_b are zero.

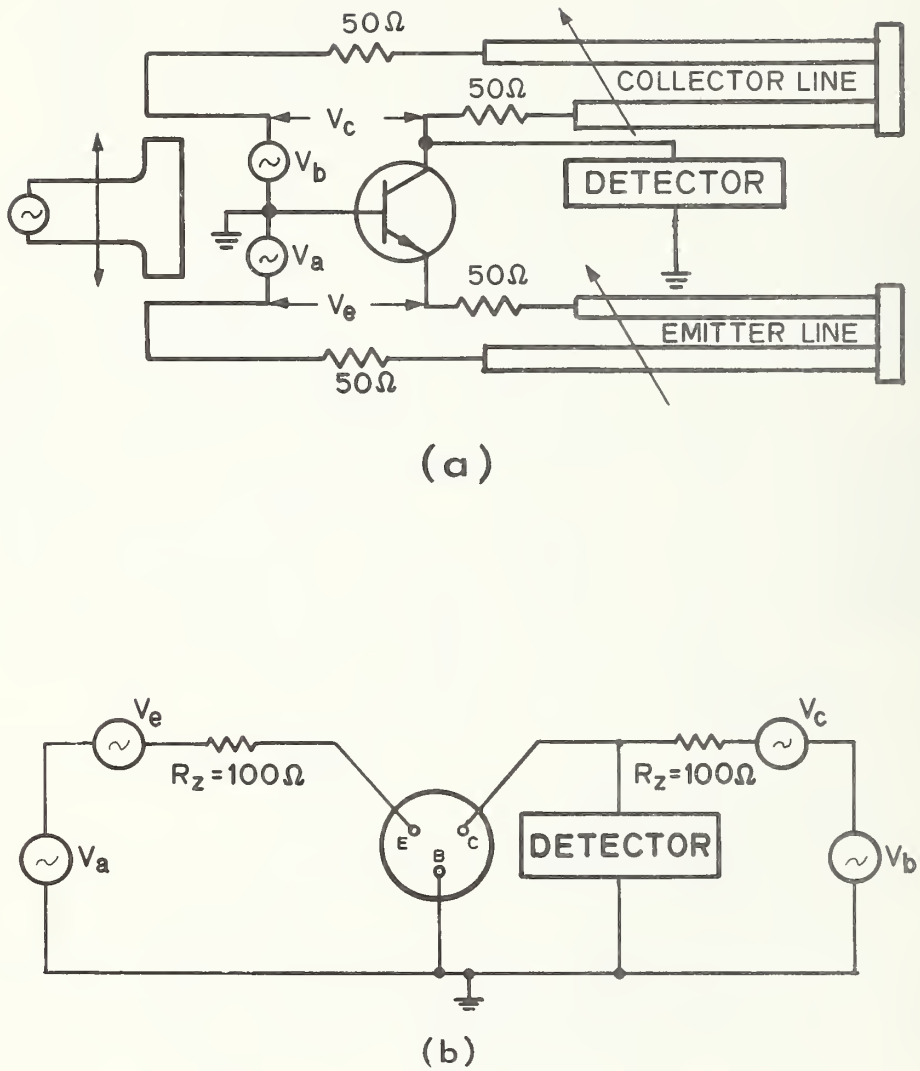

Figure 5. Sandia Bridge. (a) Circuit Diagram (b) Equivalent Circuit

The bridge is a null-type instrument and the detector input voltage is zero when a delay time value is recorded. This requires that the signals at the detector input due separately to V_e and V_c be exactly equal in magnitude and differ in phase by exactly 180 deg. The relative magnitudes are adjusted by moving the input loop closer to the emitter, or to the collector, coupling loop with a fine lead screw in the phase-splitter and attenuator box.* Phase adjustment is performed with the use of adjustable-length coaxial lines (trombones) in the emitter and collector circuits. In the NBS-constructed version, the lines were fitted with purchased scales marked in phase delay time. A technique for spot-checking the scale calibration was developed and is described in Section II 4a; the scale calibrations were found to be accurate to within 0.1% and so scale correction factors were not required.

Delay time measurements are conveniently referenced to a zero established by an emitter-collector short-circuit in the transistor socket. The bridge is balanced, then the short-circuit is removed and the transistor or other network to be measured is inserted and biased by means of power supplies not shown in figure 5. The control on the phase-splitter and attenuator box and the length of the collector coaxial line are again adjusted for a detector null. The phase delay time charged to the network in the transistor socket is the increase, relative to the emitter-collector short-circuit reference value, in delay time read on the collector trombone. The following nomenclature is adopted to facilitate the description of the use of the bridge: *indicated delay time* is the difference between the delay times read from the collector and emitter delay lines, with the emitter delay subtracted from the collector delay, *measured delay time* is the *indicated delay time* less the corresponding quantity obtained with a network consisting of an emitter-collector short and open base, while *corrected delay time* refers to

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* The phase-splitter and attenuator box is similar to that shown as figure 3 in reference 2; we are indebted to the Sandia Laboratories for providing a set of construction drawings.

the quantity obtained by adding to the *measured delay time* an appropriate correction term. The symbols are τ_I, τ_m, and τ_c, respectively.

For the transistor of figure 2 in the socket, the analysis recorded in Appendix II shows that the true measured delay time which is obtained in the absence of extraneous signal pickup is

$$\tau_t = \frac{1}{1 - \frac{\alpha(\omega)\ r_b}{R_z+r_e+r_b}} \left\{ \tau_\alpha + \left(1 - \frac{r_e}{R_z+r_e+r_b} \right) \tau_e - \tau_{bc}/h_{fe} \right\} \qquad (10)$$

where $R_z = 100\Omega$*. We note that if $R_z \to \infty$, then the above delay time expression becomes identical to the delay time expression for the vector voltmeter in equation 9. The quantities r_e, r_b and $\alpha(\omega)$ can all be determined using standard techniques and so the quantities multiplying τ_α, τ_e and τ_{bc} (which did not appear in equation 9) can be computed.

c. Influence of Extraneous Pickup at the Measurement Frequency. The measurement systems described above, as well as others such as the Das-Boothroyd bridge (reference 4) have been found to be quite useful for transistor measurements, but their accuracy may be severely compromised by the presence of extraneous signals at the measurement frequency. This is illustrated in figure 6. The vector of magnitude a at the angle θ_0 below the reference (input) axis represents the output signal from the transistor, and the vector of magnitude b represents an extraneous signal at the measurement frequency. The effects are most severe when $\vec{a}$ and $\vec{b}$ are orthogonal; for this case, in which the output signal makes an angle $\theta_\Delta << \pi/4$, b/a is approximately equal to θ_Δ and the phase delay time error due to $\vec{b}$ is $\tau_\Delta \simeq (b/a)/\omega$. If we wish to describe delay time error in terms of R, the electrical isolation, then $\tau_\Delta \simeq (1/\omega)\ [1/\text{antilog}_{10}\ (R/20]$, where -R is the ratio (b/a) expressed in decibels. Table I relates

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* R_z, the sum of the source and load impedance, is twice the characteristic impedance of the delay lines.

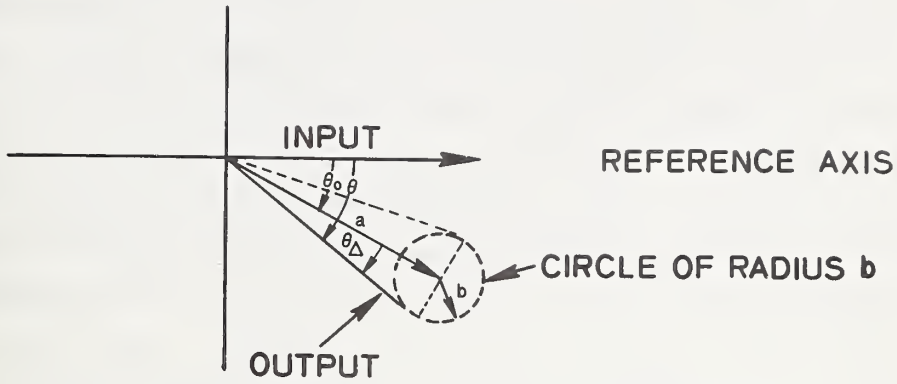

Figure 6. Diagram Illustrating The Effect Of Extraneous Pickup On The Measured Phase Angle θ For The Worst-Case Condition.

Table I

Possible Delay-Time Errors Due to a Lack of Perfect Circuit Isolation

(b/a) in dB (Isolation)	-80	-60	-40	-20
τ_Δ (ps) for $\omega/2\pi$ = 30 MHz	--	--	52	520
20 MHz	--	--	78	780
10 MHz	--	16	160	1600
5 MHz	--	32	320	3200
2 MHz	--	78	780	7800
1 MHz	16	160	1600	16,000

τ_Δ to -R for various frequencies. The conclusion to be drawn from Table I is that a high degree of circuit isolation is needed to make accurate delay-time measurements, particularly if the transistor is a high-frequency device (small delay time) and a low (1 to 10 MHz) measurement frequency is used. Some causes of extraneous coupling are direct radiation from signal source to detector, radiating cables connecting source and detector to the measurement circuit, and undesired coupling within the measurement circuit (due to ground loops, for example). The first two may be eliminated easily, but the third is more elusive. However, a method has been developed to enable one to correct for the effects of extraneous coupling on delay-time measurements. The magnitude of the error-producing sources and their locations can be found and appropriate correction terms calculated. These error-producing sources are a property of the particular measurement system, and they remain constant unless the system is changed. Once they are specified, one can greatly reduce their influence on transistor delay-time measurements.

As mentioned in Appendix II, V_a and V_b in figure 5 represent extraneous signal sources at the measurement frequency. If V_a and V_b exist, one intuitively would expect that the null condition (bridge balance) will require a different combination of the amplitudes and phases of the controlled sources V_e and V_c than are required when V_a and V_b are both zero. This change in the phase relationship between V_e and V_c may lead to delay-time measurement errors. This supposition is substantiated both by analysis and by experiment. A workable analytic approach is based on assuming n extraneous signal sources, one in each of the n connected loops making up the delay-time measurement circuit. This is the starting point for the analysis which is described in detail in Appendix II. From measurements of the delay time of n different, simple, known networks plugged into the transistor socket, it is possible to calculate the magnitude of each of the n extraneous sources. Since at balance the detector current is zero, any loop involving the detector is effectively open and so the number or extraneous signal

sources required to characterize the bridge in figure 5 is only two, rather than three.

One of the known networks chosen is simply a transistor header with a short circuit across the emitter and collector posts and a floating base lead. The other employs a resistor of value R_s connected close to the header between the emitter and collector leads; again the base lead is unconnected. The circuit of figure 5 is analyzed for each of these networks in the transistor socket. As shown in the appendix, this produces two equations in the two unknowns (V_a/V_e) and (V_b/V_e). The equations may be solved simultaneously to yield

$$\frac{V_a}{V_e} = \frac{(R_z + R_s)}{R_s}\left(\frac{V_c}{V_e}\right)_s = \frac{(R_z + R_s)}{R_s}\left(\frac{V_c}{V_e}\right)_{rs} - 1 \tag{11}$$

$$\frac{V_b}{V_e} = \frac{R_z}{R_s}\left(\frac{V_c}{V_e}\right)_s = \frac{(R_z + R_s)}{R_s}\left(\frac{V_c}{V_e}\right)_{rs} \tag{12}$$

The subscripts s and rs refer to circuit conditions which exist when the short circuit, and resistor, respectively, are used. The corresponding indicated delay times are designated τ_s and τ_{rs}. Equations 11 and 12 allow the delay time for any network of known configuration in the transistor socket to be corrected for the effects of the error-producing sources V_a and V_b.

(1) Confirmation of Theory by Measurements on R-C Networks. Discrete elements were assembled as described in Section II 3 on a transistor header to form the network represented by figure 1. The resistors are of equal value; $R_1 = R_2 \equiv R$. With the network in the circuit shown in figure 5, Appendix II shows that the following equation is obtained at bridge balance:

$$\frac{V_c}{V_e} = \frac{R_z}{(R_z+2R)\ [1+j\omega RC\ \ (R_z+R)/(R_z+2R)\ ]} \tag{13}$$

$$+\ \frac{V_a}{V_e}\ \frac{R_z}{(R_z+2R)\ [1+j\omega RC\ \ ((R_z+R)/(R_z+2R))\ ]}\ -\ \frac{V_b}{V_e}$$

The left-hand side of equation 13 can be written as

$$\frac{V_c}{V_e} = \left|\frac{V_c}{V_e}\right| e^{-j\omega\tau_I} \tag{14}$$

to put this equation in the same form as equation 1 and to allow us to identify τ_{ph} in equation 2 with the indicated delay time τ_I for the R-C network. With $\omega RC << 1$, as is the case for the R-C network over the frequency range used, and with V_a and V_b each smaller* than V_c, equating the imaginary components of equation 13 yields the indicated delay time

$$\tau_I = \tau_{RC}\ \frac{(R_z+R)}{(R_z+2R)} + \frac{j}{\omega}\ Im\ (\frac{V_a}{V_e})\ -\ \frac{(R_z+2R)}{R_z}\ \frac{j}{\omega}\ Im\ (\frac{V_b}{V_e}) \tag{13a}$$

where $RC \equiv \tau_{RC}$.

In terms of the measured delay time $\tau_m = \tau_I - \tau_s$, equation 13a becomes

$$\tau_m = \tau_{RC}\ \frac{(R_z+R)}{(R_z+2R)} - \frac{2R}{R_z}\ \frac{j}{\omega}\ Im\left(\frac{V_b}{V_e}\right) \tag{13b}$$

and shows that use of an emitter-collector short circuit to establish the delay time zero eliminates the effects of V_a, the extraneous signal generator in the emitter-base loop, on delay-time measurements of networks

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* This assumption is expected to hold quite well for any bridge constructed with reasonable care.

such as shown in figure 1. This seems to be a general result which holds for all networks, including transistors, investigated to date.

Figure 7 shows plots of $\frac{j}{\omega}\ Im\ (Va/Ve)$ and $\frac{j}{\omega}\ Im\ (Vb/Ve)$ as a function of frequency for the NBS version of the Sandia bridge. To cancel the error in the measurement of the R-C networks due to the extraneous signal generators and leave simply $\tau_{RC}\ (R_z+R)/(R_z+2R)$, we would add to the recorded delay time a correction term which is the negative of either the last two terms in equation 13a or the last term in 13b, depending on the measurement technique. This is equivalent to canceling out the effects of the extraneous signal sources. It should be noted that in neither case does the correction term depend on the delay time of the R-C network.

The graphical correction may be tedious and may suffer from inaccuracies since it requires that a curve, or a set of curves, first be drawn and read. An alternative and completely equivalent correction method is based on recording the indicated delay times τ_s and τ_{rs} at the frequencies and at about the same times as network delay time values are recorded and making the corrections in terms of τ_s and τ_{rs}. From equations 11 and 12,

$$\frac{j}{\omega}\ Im\left(\frac{V_a}{V_e}\right) = \frac{(R_z+R_s)}{R_s}\ \tau_s - \frac{R_z}{R_s}\ \tau_{rs}, \text{ and} \tag{11a}$$

$$\frac{j}{\omega}\ Im\ \left(\frac{V_b}{V_e}\right) = \frac{R_z}{R_s}\ \tau_s - \frac{R_z}{R_s}\ \tau_{rs} \tag{12a}$$

inserting these into equation 13a,

$$\tau_I = \tau_{RC}\ \frac{(R_z+R)}{(R_z+2R)} - \frac{(2R-R_s)}{R_s}\ \tau_s + \frac{2R}{R_s}\ \tau_{rs} \tag{15}$$

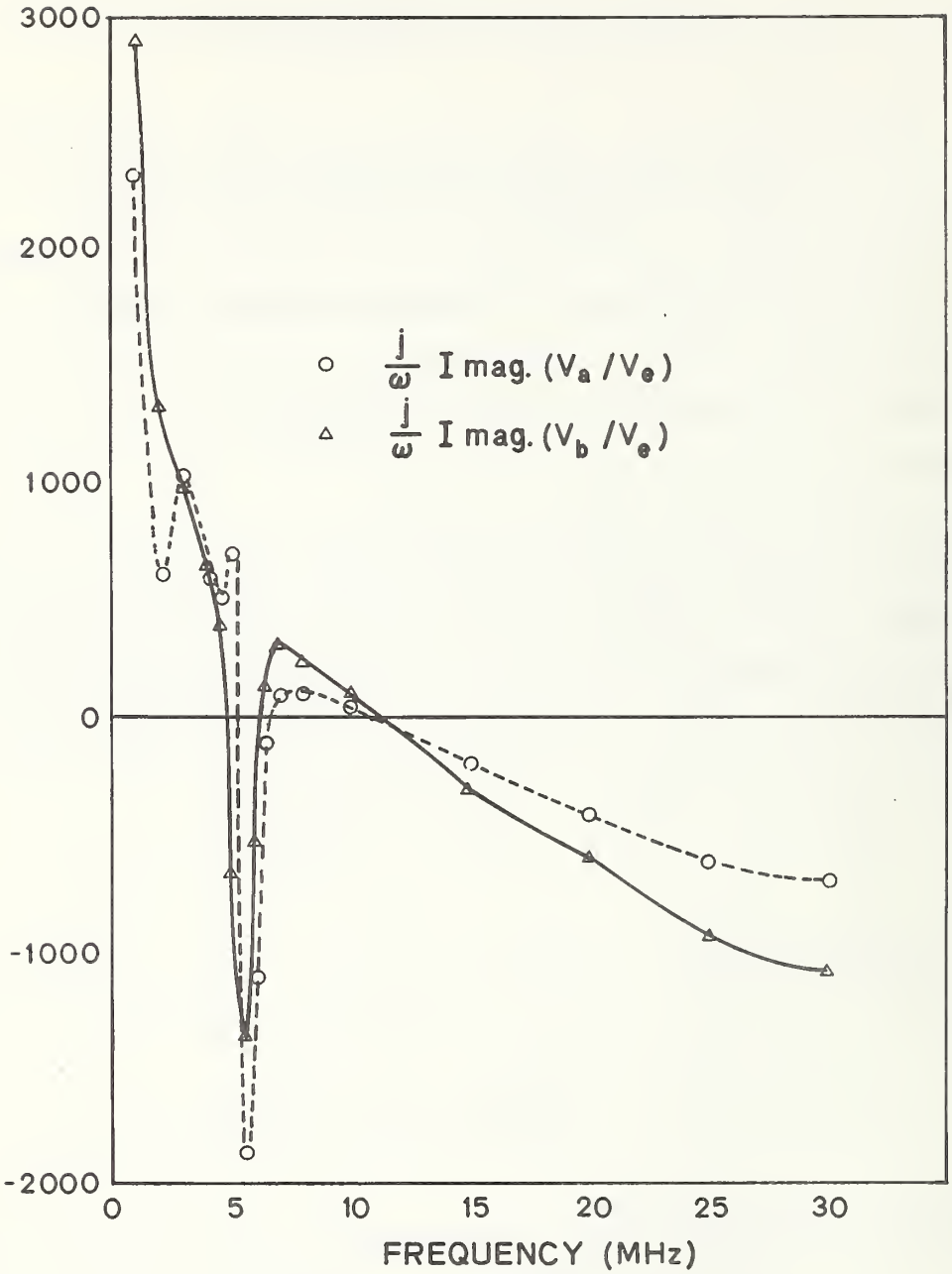

Figure 7. Plots $\frac{j}{\omega} Im\left(\frac{V_a}{V_e}\right)$ and $\frac{j}{\omega} Im\left(\frac{V_b}{V_e}\right)$ As a Function of Frequency For The NBS Version Of The Sandia Bridge.

Alternatively, by analogy with equation 13b, combining equation 11a, 12a, and 13a, the measured delay time is

$$\tau_m = \tau_I - \tau_s = \tau_{RC} \frac{(R_z+R)}{(R_z+2R)} - \frac{2R}{R_s} (\tau_s - \tau_{rs}) \qquad (15a)$$

Of the four delay-time expressions for the R-C network, equation 15a is the simplest, and hence probably the most useful. The correction term is proportional to the shift in indicated delay time zero when the emitter-collector short circuit is replaced by a resistor of value R_s. Since equation 15a is the analogue of equation 13b, only the extraneous signal generator in the collector-base loop, V_b, contributes to measurement error. Although the constant of proportionality in the correction term varies with the value of R for the R-C network, it does not involve the capacitance C, and so it does not depend on the time constant of the network. Furthermore there are no adjustable constants in the correction term $(2R/R_s)$ $(\tau_s - \tau_{rs})$; all the parameters are fixed.

Tests of the above delay-time expression were made using several R-C plug-in networks. The data on network N4, which had a time constant of 655 ps (R = 10.33 Ω and C = 64.6 pf) shown in figure 9, are representative of the results of these tests. Curve A is the measured delay time. The value R_s = 20 Ω ≃ 2R was chosen for the measurement of τ_{rs}, and so the correction term is simply $(\tau_s - \tau_{rs})$. Curve B, the corrected delay time, is the sum of the measured delay time, curve A, and the correction term, and is sensibly independent of frequency, as it should be.

(2) Correction of Transistor Delay time Measurements

The procedure developed above can be used to correct the measured delay time of any network of known composition. Before applying the method to transistors it is profitable to discuss the implications of V_a and V_b on delay-time measurements. It is apparent that V_a has no effect if the reference measurement condition is an emitter-collector short circuit. Under the same conditions, however, V_b can cause measurement inaccuracies unless

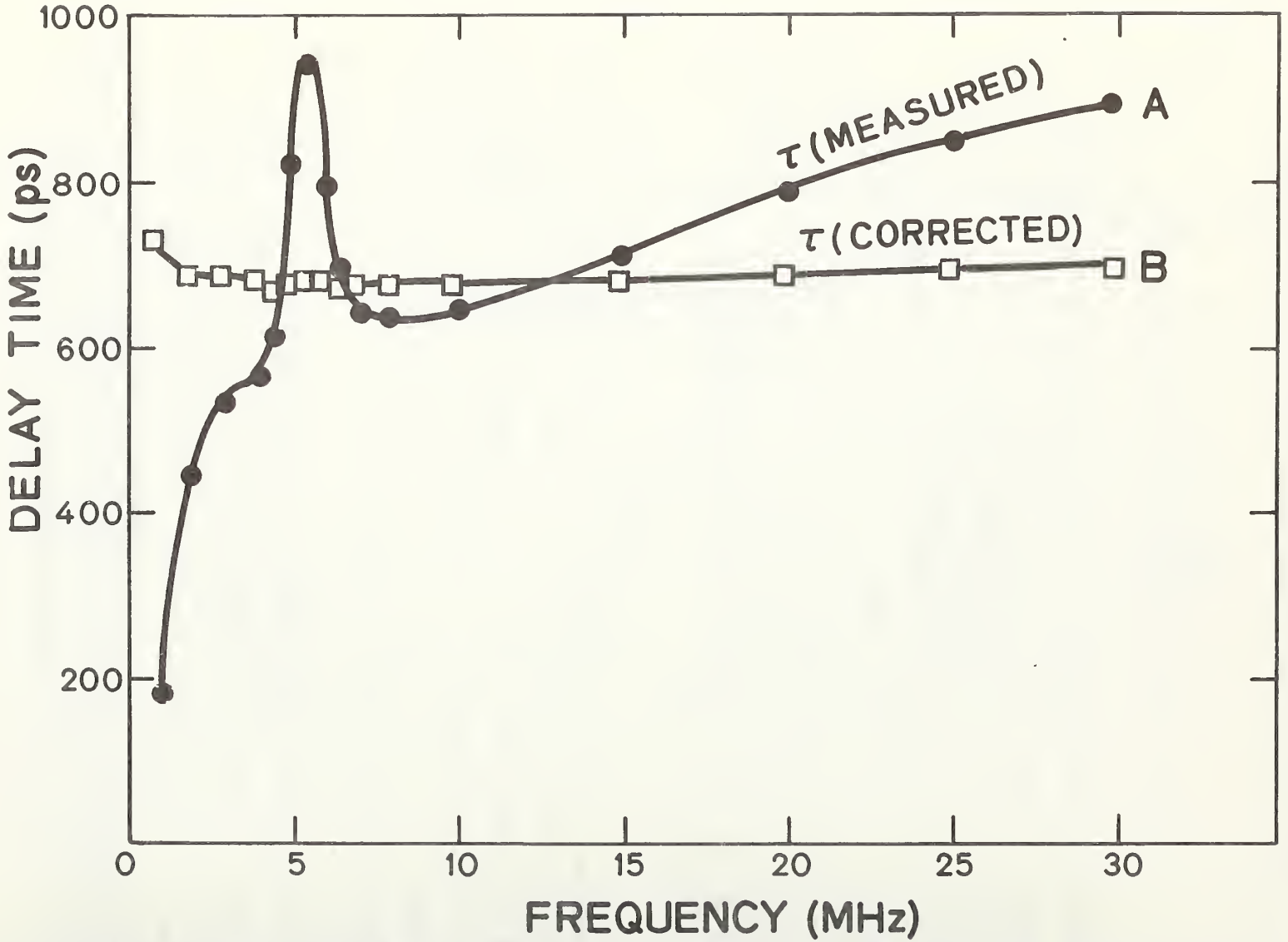

Figure 8. Correction of Delay Time for Plug-In Network N4. The Curve A Is The Measured Delay Time While B Is Obtained By Adding To A The Independently-Obtained Quantity Given By The Last Term On The Right-Hand Side Of Equation 15a.

the proper correction term is found and added to the measured delay time. All of this can be brought into perspective if we first consider the case of a lossless network in the transistor socket, and later allow the network to attenuate the signal current in its emitter circuit. The initially lossless network can only contribute a phase shift between the E and C terminals (See figure 5). As there is no base current, the bridge circuit degenerates to one having but a single loop, and the effects of the separate sources V_a and V_b are those of the sum of these sources; the equivalent source is a single one and may be placed in the emitter lead, and measurements made relative to an emitter-collector short circuit will be unaffected by this equivalent source. This means that the measured delay times of networks having vanishingly small base currents, networks in which the equivalent circuit approaches that of a single loop excluding the base terminal, will not be influenced by extraneous signal sources. However, if for a given, initially lossless, network the base current is increased by any cause, the measured delay time becomes susceptible to the influence of the collector-base extraneous generator V_b. The effect of V_b on delay-time measurements will be larger, the larger the base current. This phenomenon may be quite important as when transistor measurements are made after h_{fe} degradation such as occurs when transistors are irradiated with neutrons. Then the measured delay time can change significantly and show a marked frequency dependence. However, if the equivalent circuit of the transistor is known, it is a straightforward matter to obtain a correction for the delay time measured after gain reduction. In the absence of this correction, erroneous conclusions may be reached as to the effects of the radiation on the devices under test.

For the transistor represented by figure 2 the measured delay time is (see Appendix II)

$$\tau_m = \tau_t - \left(\frac{1}{hfe} \frac{(R_z + r_b + r_e)}{R_z} + \frac{r_e}{R_z} \right) \frac{j}{\omega} Im \left(\frac{V_b}{V_e} \right) \qquad (16)$$

where τ_t is the delay time (equation 10) which would be obtained from the bridge in the absence of extraneous signal pickup. The correction term, τ_c is seen to be

$$\tau_c = \left(\frac{1}{h_{fe}} \frac{(R_z + r_b + r_e)}{R_z} + \frac{r_e}{R_z} \right) \frac{j}{\omega} Im \left(\frac{V_b}{V_e} \right) \tag{17}$$

which may also be derived in terms of the delay-time zero shift $(\tau_s - \tau_{rs})$:

$$\tau_c = \left(\frac{1}{h_{fe}} \frac{(R_z + r_b + r_e)}{R_s} + \frac{r_e}{R_s} \right) (\tau_s - \tau_{rs}) \tag{17a}$$

3. R-C NETWORKS

From the analysis, it can be seen that R-C elements suitably combined on transistor headers provide a means for checking delay time instruments. Furthermore, these networks also provide a convenient, and very portable, means for spot-checking the calibration of various delay-time measurement systems. Several networks of the type shown in figure 1a were assembled on transistor headers to provide delay times between 100 and 1,000 ps. The electrical circuit consists of two metal-film-on-ceramic resistors of equal value R and a porcelain capacitor of value C as shown in figure 9. The resistors were mounted on 2.5-mm-high ceramic posts to reduce stray capacitance to the header and were connected between the common point of the two resistors and the header, which was also connected to the base pin. The header connection was made with a conducting epoxy, and 1-mil (0.025 mm) diameter gold wires were thermocompression bonded to interconnect the capacitor and the resistors and connect the resistors to the emitter and collector pins. Table II lists the R and C values for networks N1 through N4. S-Parameter measurements show that the resonant frequencies for these networks are well beyond the 2 to 30-MHz operating frequency range of both the Sandia bridge and vector voltmeter delay time instruments. Later versions

Figure 9. Photograph of an R-C Delay Time Network Having The Circuit Shown In Figure 1a.

were developed which are non-resonant below 2 GHz. The parasitic inductance in these networks, which are also suitable for the intercomparison of transistor S-parameter systems in the 0.1 to 2.0-GHz range, was reduced by eliminating the fine gold wires: the components were arranged to butt the proper electrodes together with a conducting epoxy film between the butting surfaces.

Table II

Tabulation of Resistance and Capacitance Values for Four R-C Delay-Time Networks

Network	$\tau_{ph} = R_2C_1$ (ps)	$R_1 = R_2$ (Ω)	C_1 (pf)
N1	212	2.26	93.8
N2	504	2.29	220.0
N3	202	10.32	19.6
N4	665	10.33	64.4

4. EQUIPMENT CALIBRATION AND USE

a. Vector Voltmeter

The block diagram of the vector voltmeter delay time apparatus and the schematic diagram of its transistor test fixture were shown and briefly discussed in Section II. The present section is concerned with the calibration of the apparatus and with suggestions for its use.

Equation 2 shows that both the measurement frequency and the phase angle must be known accurately if one is to accurately compute phase delay time from vector voltmeter measurements. The frequency can be measured accurately with a suitable frequency counter, but ensuring an accurate calibration of the vector voltmeter phase meter is more difficult. The circuit in figure 10 was assembled to satisfy this calibration need. The characteristic impedance is 50 Ω, and all connections were made with coaxial cables or rigid coaxial lines. The constant impedance, variable-length trombone

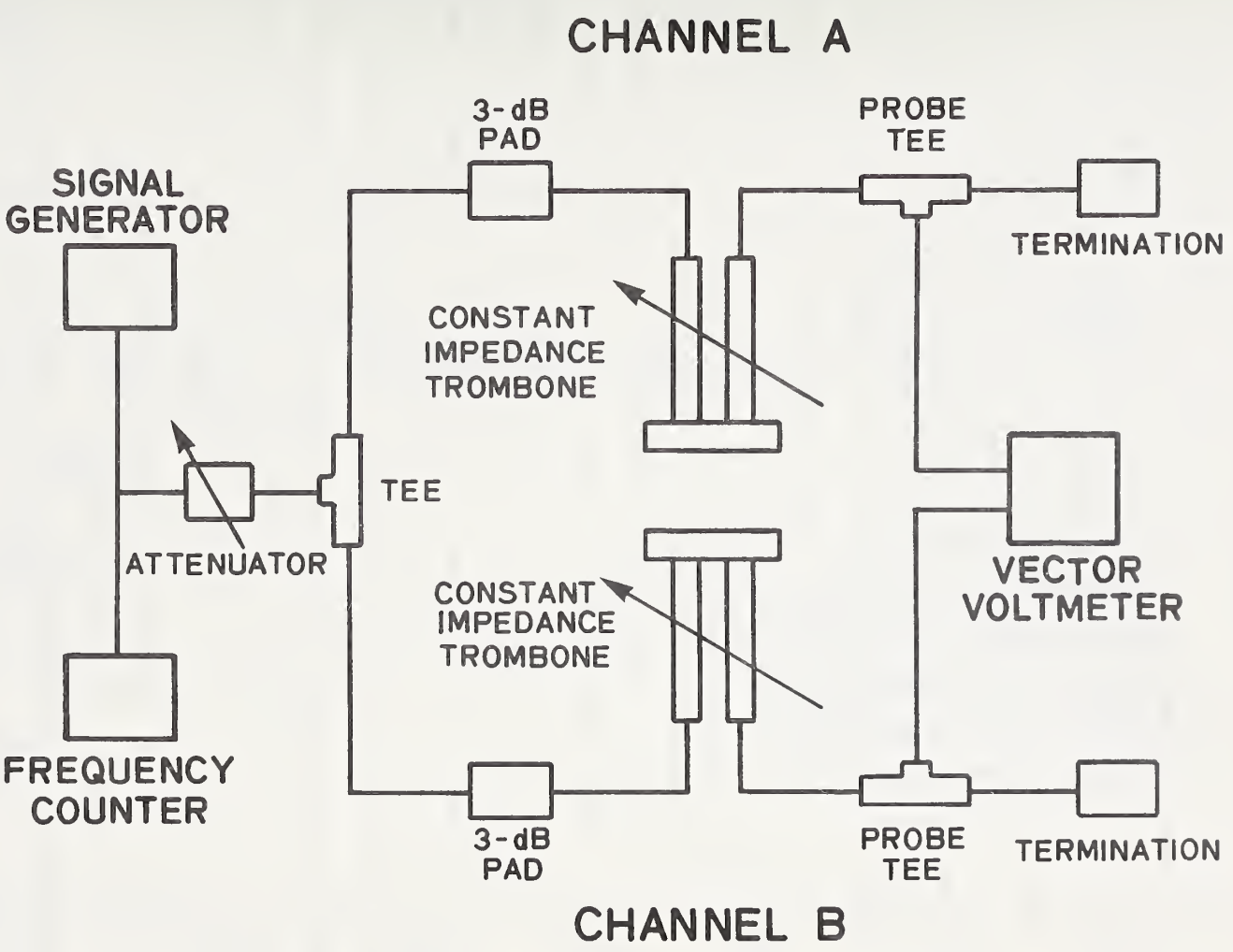

Figure 10. Circuit For The Calibration Of The Vector Voltmeter Phase Meter

lines used in the Sandia bridge were used to provide known values of phase delay. Their scale calibrations were checked by placing a convenient length of air line in channel A and connecting both trombones in series in channel B. With both trombones collapsed, a sinewave signal of 400 MHz was applied and the vector voltmeter phase angle noted. The trombones were then varied to shift the phase by exactly 360 deg so that the phase angle previously noted was restored. Then the sum of the incremental delay times read on the trombone scales should be equal exactly to 2.5 ns, the reciprocal of the test frequency. It should be noted that this result is independent of the calibration of the vector voltmeter as the only requirement placed on it is that the reading be the same before and after the trombones are adjusted. The measurement was repeated several times for trombone settings in the range 1 to 1.5 ns; the total delay times measured were slightly larger than, but always within 2 ps (0.1%) of the reciprocal of the test frequency. With the trombone accuracy verified, they now may be used in the circuit of figure 10 to determine the accuracy of the calibration of the phasemeter in the vector voltmeter. Measurements were made at frequencies between 2.777 and 27.77 MHz. Three ranges of signal amplitude, 0.4 to 1.0 mV, 4.1 to 7.8 mV, and 44.0 to 65.0 mV, as read on the vector voltmeter, were used at each frequency. Measurements were made both for leading and lagging phase angles between 0 and 6 degrees, a range expected to encompass almost all of the transistors to be measured. The phase of A was taken as the reference established by the vector voltmeter. The phase angles computed from the trombone settings were divided by the angles read on the phase meter, and these ratios were plotted as a function of the angle read for the various frequencies, and for the three amplitude ranges. Figure 11 shows the results for the highest signal range, and figure 12 shows results for the lowest. The signal amplitude for the latter was chosen to be only a factor of three or four greater than the operating threshold for the instrument, and in this lower operating range, the phase-meter is not steady but jumps around, much as a noise signal would. The conclusion to be drawn from these figures is that the phase angle presentation is low by about 3 percent, and is not a strong function of frequency and amplitude over the ranges of interest.

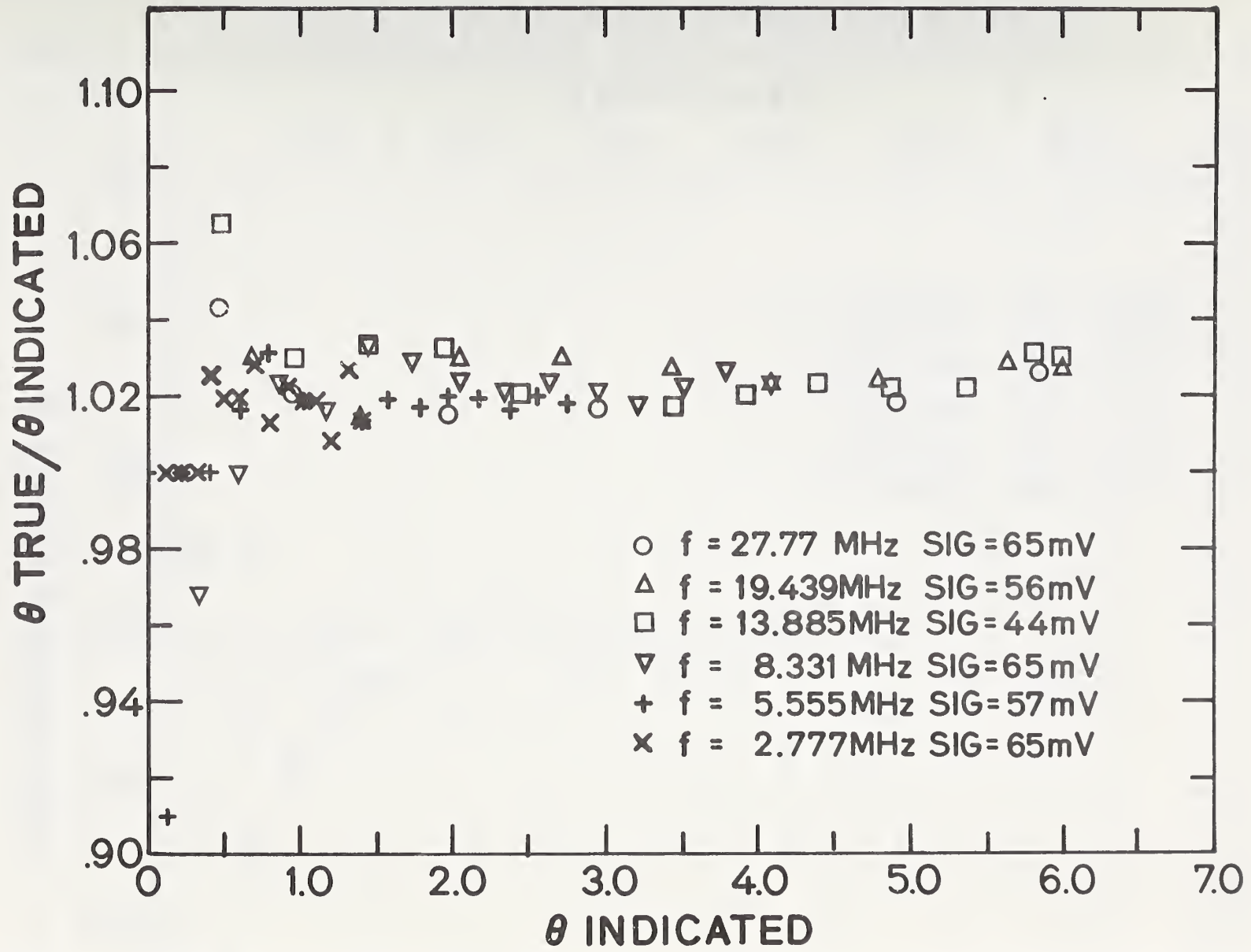

Figure 11. Values of θtrue/θindicated Plotted Against θindicated For Various Frequencies From 2.777 to 27.77 MHz And With Signal Amplitudes From 44 to 65 mV.

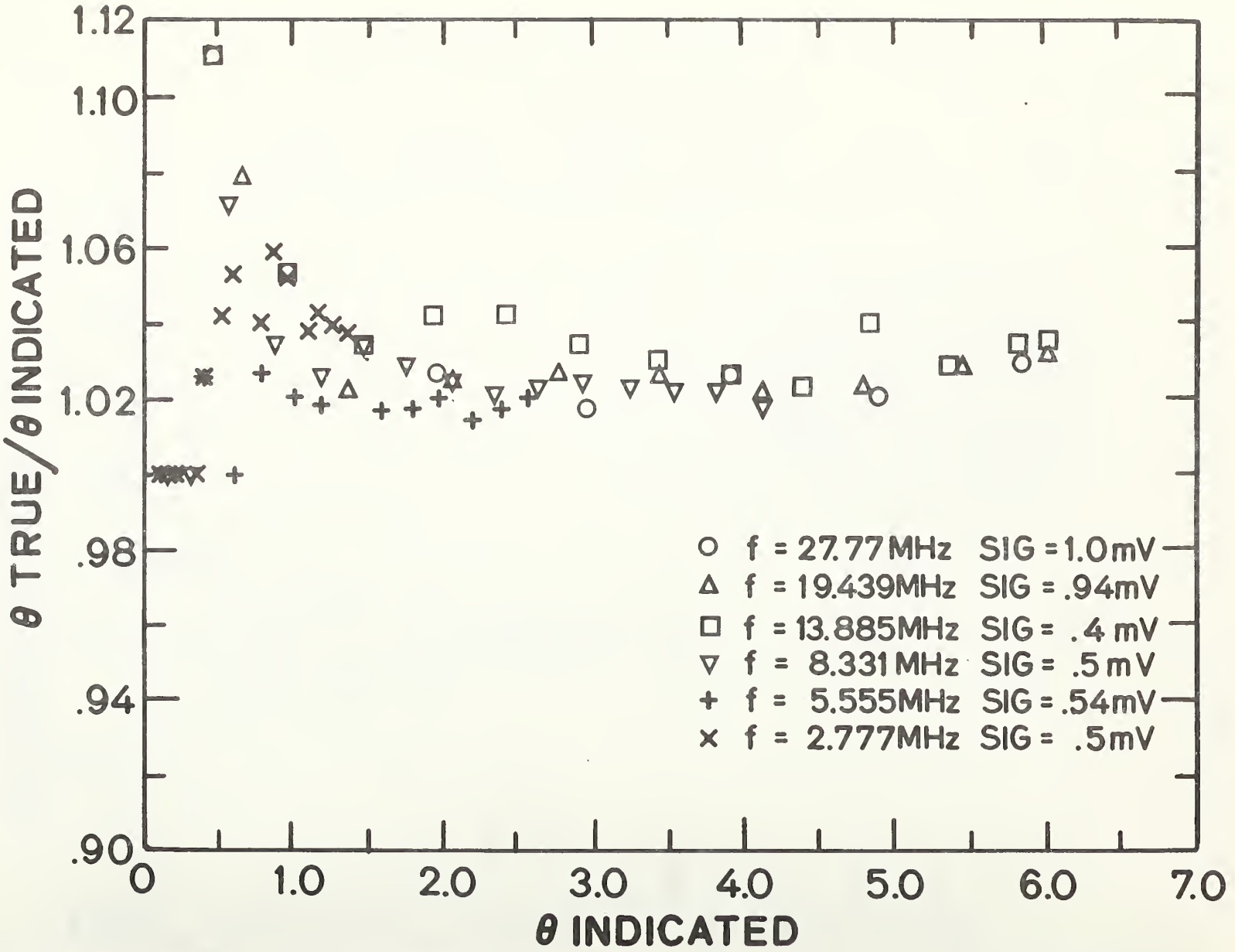

Figure 12. Values Of θtrue/θindicated Plotted Against θindicated For Various Frequencies From 2.777 To 27.77 MHz And With Signal Amplitudes From 0.4 To 1.0 mV.

With this known, it is a simple matter to correct the phase-meter reading by multiplying by an appropriate factor the observed phase angle to obtain the true phase angle between channels A and B.

To establish a delay time zero reference for transistor measurements, an emitter-collector short-circuit is inserted into the transistor socket and the phase meter is set to zero with the control on the front panel of the vector voltmeter. On some vector voltmeters the zero reference may vary slightly with the A-channel (reference) signal amplitude. Whether or not this is true for a particular instrument may be ascertained quite simply with the short-circuit in the socket by varying the amplitude of the signal to the transistor test fixture over the range normally used. If the phase-meter zero changes, then both the zero setting and transistor measurements must be made with the same A-channel signal amplitude.

Measurements are made by replacing the emitter-collector short circuit with the network or transistor to be measured, suitably biasing the transistor, and interpreting the resulting phase angle in terms of delay time as outlined in Section II 1. It is important that small-signal conditions be employed for transistor measurements since erroneous delay time values may be expected if these conditions are violated. Use of amplifiers between the current probes on the transistor test fixture and the vector voltmeter ensures that the signals to the vector voltmeter are large enough for its operation, while permitting the transistor to be measured under small-signal conditions. To test for small-signal operation, the signal attenuator in figure 3 is used to decrease the signal to the test fixture to about one-half of its previous value. If the delay time now measured agrees within the allowable measurement error with that recorded for the previous, larger input signal, then the signal amplitude can be assumed to be within the small-signal range. An alternate test is to double the input signal and to compare the resulting delay time with that previously recorded.

Ideally, delay times for transistors should be independent of frequency provided, as discussed in Appendix I, that the transistor time constants are much smaller than the reciprocal of the highest angular frequency used

for the measurement. For the vector voltmeter apparatus constructed at NBS and shown in figures 3 and 4, no frequency dependence is generally observed when measurements are made on small-signal, high-frequency devices. Measurements on R-C plug-in networks described in Appendix I show that frequency dependence, when it is observed for these units, can be accounted for by the presence of parasitic inductance in the collector-base loop of the transistor fixture, which, together with the capacitance, results in a resonant frequency near the range of the measurement frequency. These results suggest that, to a first approximation, this particular system is free from the error-producing effects of extraneous pickup. Transistors with internal capacitances larger than those currently measured may show a frequency-dependent delay time if the resonant frequency of the transistor collector-base capacitance and the parasitic inductance across the collector-base pins of the transistor socket is near the measurement frequency. From a knowledge of the value of the parasitic inductance, which may be obtained using techniques described in Appendix I, and the values of the passive elements of the transistor, the delay-time contribution from this source may be computed and thus the value observed may be corrected. For example, for the NBS-constructed version of the vector voltmeter system, equation 34 in Appendix I shows that the measured delay time is increased by an amount τ_{bc} times $[(f_o/f)^2-1]^{-1}$ where f_o is the resonant frequency of the collector-base transistor capacitance and the inductance in the test fixture (figure 4) across the collector-base pins (45.5 nH). Appendix I shows that the measured delay time for devices with small values of r_b and C_c are expected to be independent of frequency over the 2 to 30 MHz measurement range.

b. Sandia Bridge.

We have described calibration of the trombones used with the Sandia bridge to read delay time and techniques for generating the appropriate factors and terms to correct for both the finite bridge impedance R_z and the possible presence of error-producing signal sources. However, before one may properly use previously tabulated correction values, one must be sure that the system has not changed and invalidated the data. A stable system can be achieved only if care is taken with bridge construction. For the NBS Sandia bridge,

all the components with the exception of the bias sources and the signal generator and receiver are mounted on a half-inch thick sheet of composition board for portability. The bridge circuit, which consists of an input transformer, the phase-splitter and attenuator box, the set of adjustable trombone lines, and a small chassis containing the transistor socket and detector connector is joined together with locking coaxial connectors for rigidity. All coaxial lines are rigid, with the exception of the cable from the signal generator and the cable to the detector.

The input transformer serves two functions: 1) it improves the impedance match between the 50-Ω signal generator and the input loop in the phase-splitter and attenuator box, and 2) it transforms the single-ended signal generator to produce a balanced signal at the input loop. The transformer has a toroidal ferrite core. The primary consists of 20 turns of No. 30-enamel-covered copper wire and the secondary consists of 3 turns of the same size wire. A high-permeability metal shield surrounds the toroid, and the shielded assembly is enclosed in an aluminum box fitted with coaxial connectors. The detector is a communications receiver.

Occasionally transistors, particularly high-gain, high-frequency units, oscillate in the test socket. Oscillation may be evidenced by jumps in delay-time as the bias is changed or by sudden changes in the detected signal as the trombones are varied. In many cases, oscillation may be eliminated by short circuiting for ac the transistor collector to its base. This may be done with a current amplifier (an amplifier with a low impedance input) between the collector of the transistor under test and the detector. The collector to base signal voltage is zero at bridge balance, and so such a short circuit is not deleterious. The circuit of the current amplifier constructed at NBS for use with the Sandia bridge is shown* in figure 13. The input impedance is 6 Ω, and the transimpedance at 2 MHz is 250 Ω. The variation in transimpedance with frequency, referred to the 2-MHz value, was measured to 50 MHz, well beyond the highest frequency used by us for bridge operation. The results of

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* This circuit is modified from a circuit diagram received from Sandia Laboratories.

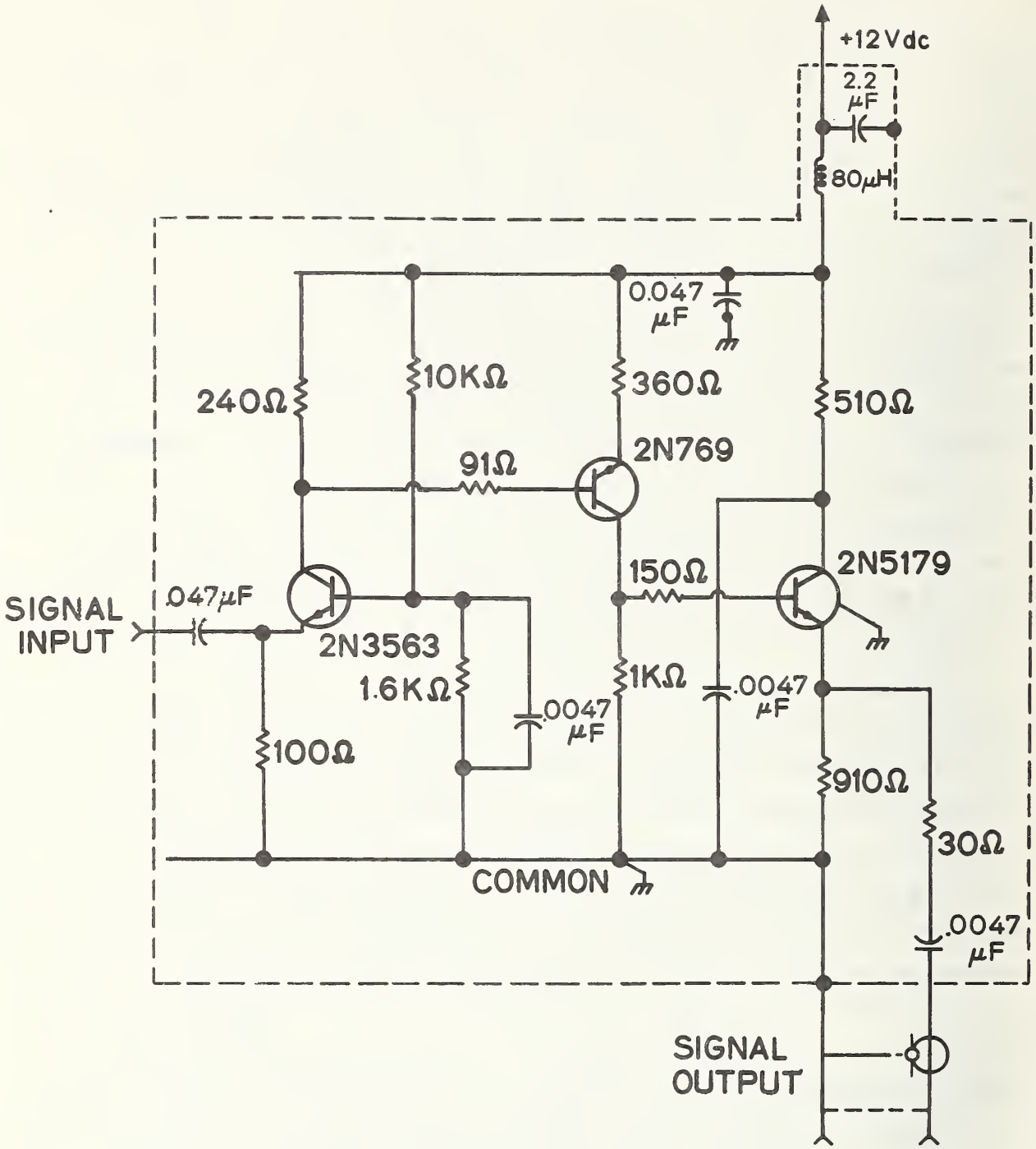

Figure 13. Schematic Diagram Of The Current Amplifier Used With The Sandia Bridge

these measurements are shown in figure 14.

5. TRANSISTOR DELAY-TIME INTERCOMPARISON MEASUREMENTS

During the early phase of the work, the delay times of several types of low-power silicon transistors were measured on both the Sandia bridge and vector voltmeter systems to compare the results obtained by these two instruments. In addition, measurements of delay times on several special high-frequency devices supplied by another laboratory were made on two Sandia bridges, one at NBS and the other at the other laboratory.

The in-house intercomparisons were made on 2N2219, 2N2222, and 2N2907A transistors. The first two are *npn* transistors while the last is a *pnp* transistor. All have power dissipation ratings less than 1 W. Delay-time measurements were made on both systems at frequencies between 3 and 30 MHz for emitter currents up to about 50 mA at a constant collector-base voltage of 5 V. For a given transistor and test frequency, the delay time measured with either system decreased with current in the manner which would be expected (see Section II 2). However, the Sandia bridge consistently measured larger delay times than the vector voltmeter system for all devices. Typically, the Sandia bridge yielded values at 10 MHz that were higher for a 2N2219 by 29 percent; for a 2N2222 by 37 percent, and for a 2N2907A by 17 percent. The origin of these differences is not known at present. Occasionally, delay times measured with the Sandia bridge revealed a significant frequency-dependence such as shown in figure 15. Such a frequency-dependence is to be expected if the transistor h_{fe} is low, and if an extraneous signal generator exists in the base-collector loop of the equivalent circuit (see Section II 2). The manufacturer states that h_{fe} values may range from 50 to 300, and this particular device may have been a low-h_{fe} sport. Unfortunately, the transistor was accidently destroyed during subsequent measurements, and so its h_{fe} could not be measured to confirm that this was the cause of the frequency-dependent behavior in this case. However, more recent measurements indicate that pronounced frequency dependence such as shown in figure 15 can be obtained from the particular apparatus used if the value of h_{fe} is 10 or lower.

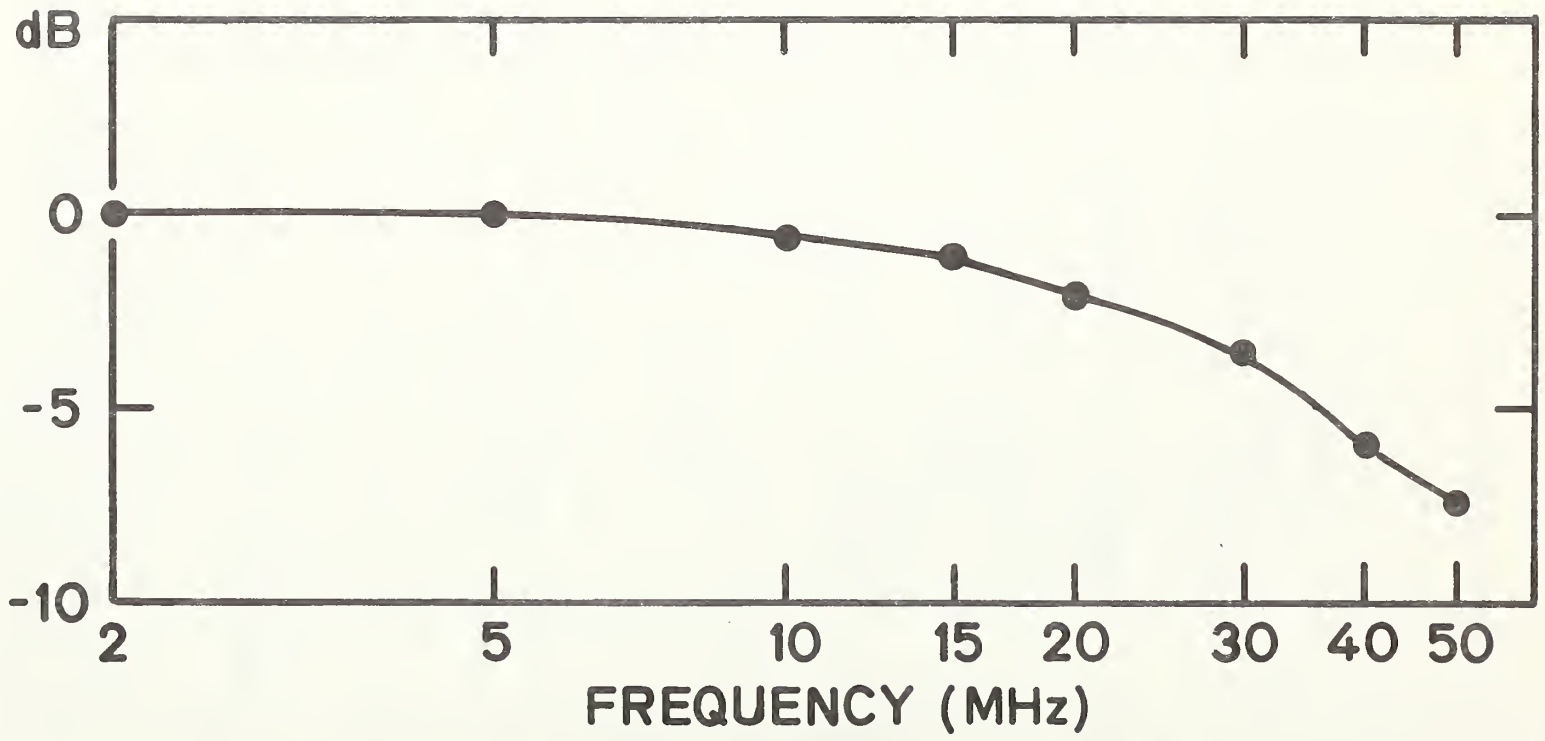

Figure 14. The Variation With Frequency of the Transimpedance of the Current Amplifier Diagrammed in Figure 13.

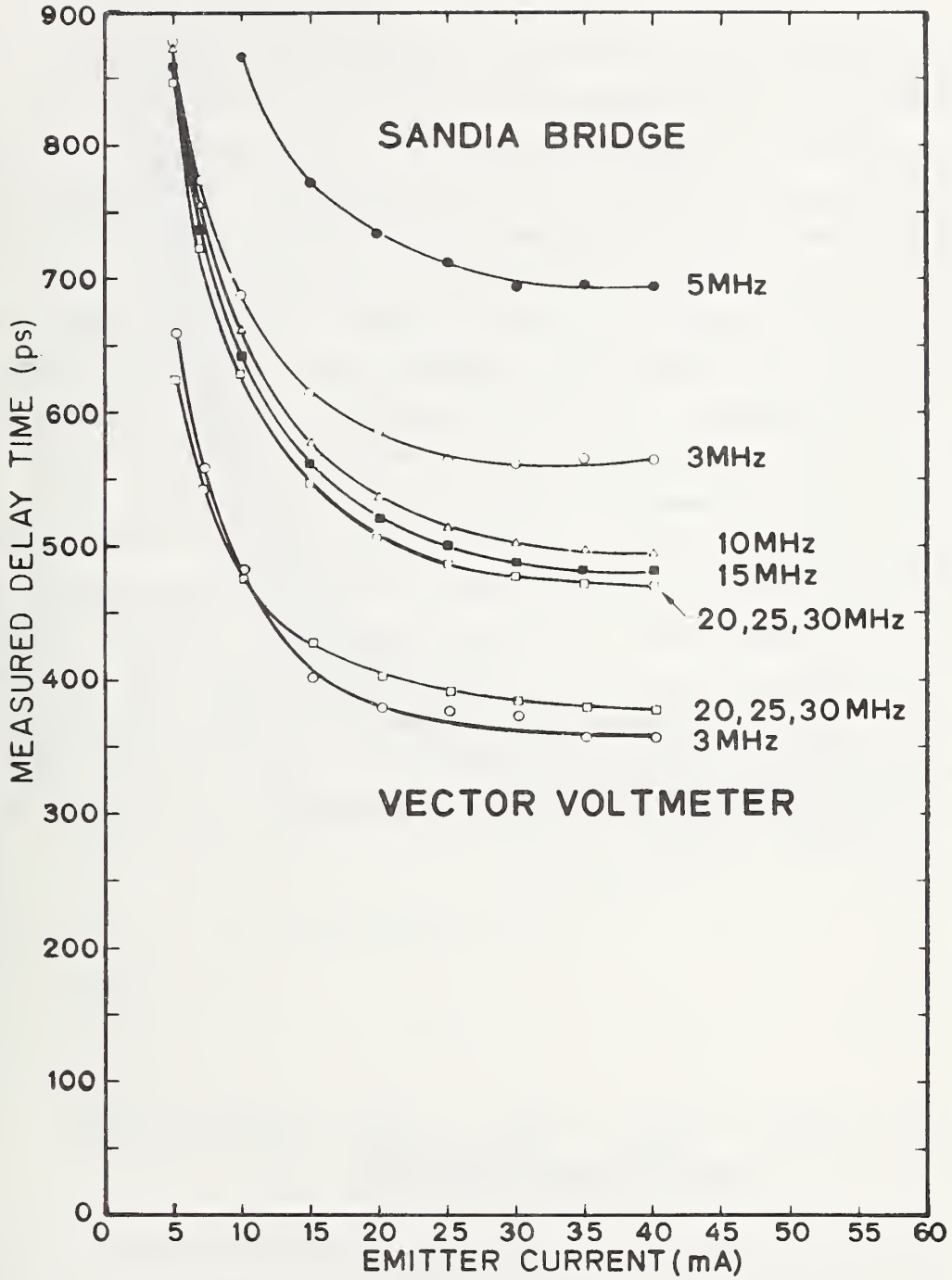

Figure 15. Delay Time of a 2N2219 Transistor Measured With a Sandia Bridge and With a Vector Voltmeter Apparatus.

The results of the interlaboratory study are shown in figures 16 and 17 for two special transistors measured with a collector-base voltage of 1.V. At NBS, delay times were measured over a range of frequencies while at the other laboratory the measurements were made only at 10 MHz. Both transistors exhibited h_{fe} values greater than 150. This may explain why the delay times measured at NBS are relatively independent of frequency between 3 and 30 MHz even though the equipment was the same as that used for the measurements shown in figure 15. The two Sandia bridges have somewhat different socket arrangements, and in each case the location of the pick-off point for the null detector was selected in such a way as to least affect the measurements. In the NBS measurements, it was found that with the pick-off point on the position of the transistor collector lead (about 2.5 mm long) between the transistor can and the socket, the delay time was 25 ps shorter than the value measured with the pick-off point at the collector socket lug. The NBS values plotted in figures 16 and 17 were measured at the former point and are believed to better represent the delay time of the transistor because the inductive contribution from the socket pin is minimized. The agreement between the in-house and the out-house systems is noticeably better for device SA 1877, figure 16, than device SA 1726, figure 17, although both could be considered as quite good for devices with such small delay times.

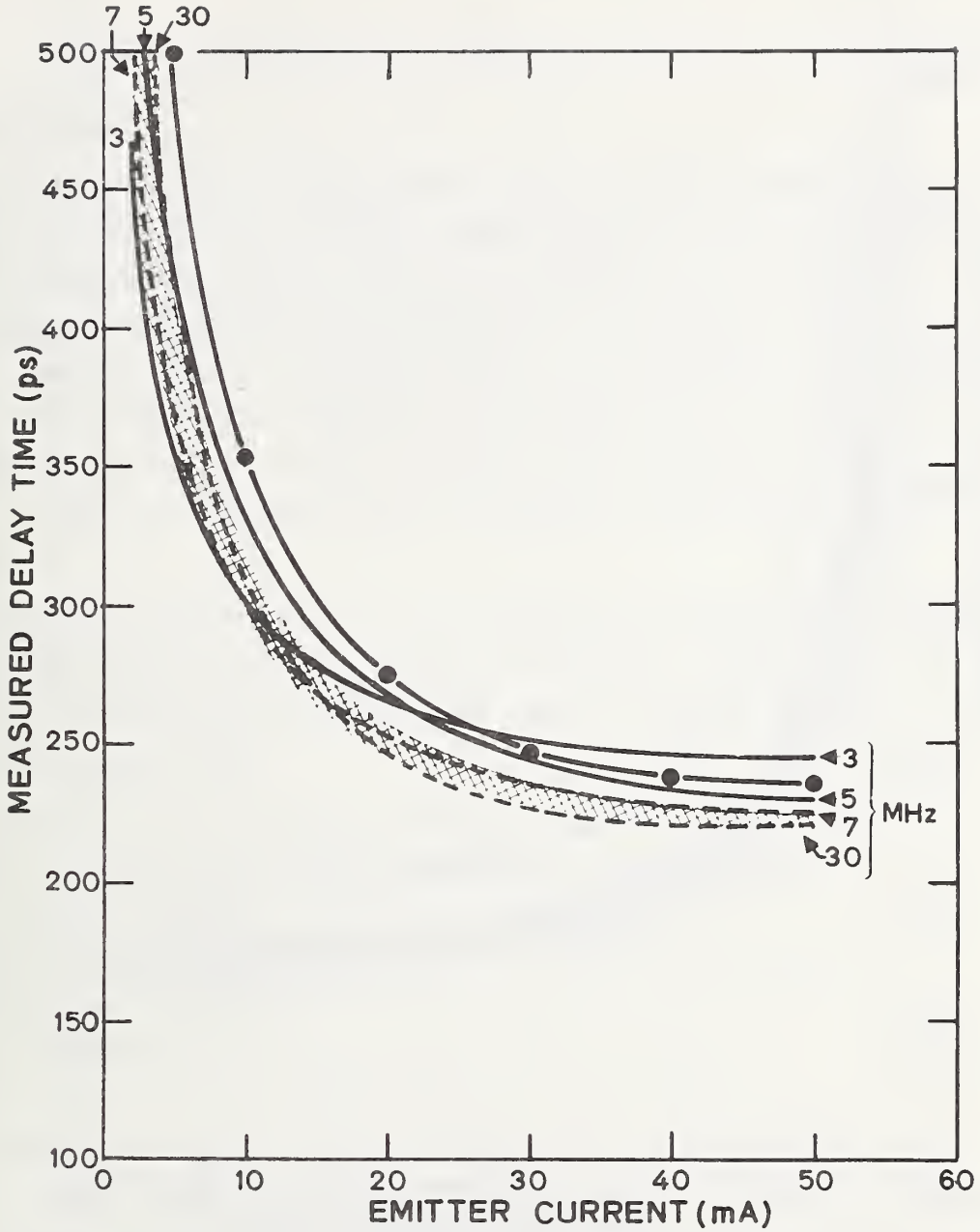

Figure 16. Results Of Interlaboratory Comparisons Of Delay Time Measurements Made With Two Sandia Bridges On a Special High-frequency Transistor. The NBS Values Measured Between 7 and 30 MHz Lie Within The Cross-hatched Area. The NBS Measurements Were Made At Frequencies Between 3 and 30 Mhz, While Measurements Made At The Other Laboratory, Shown With Circles, Were Made at 10 MHz.

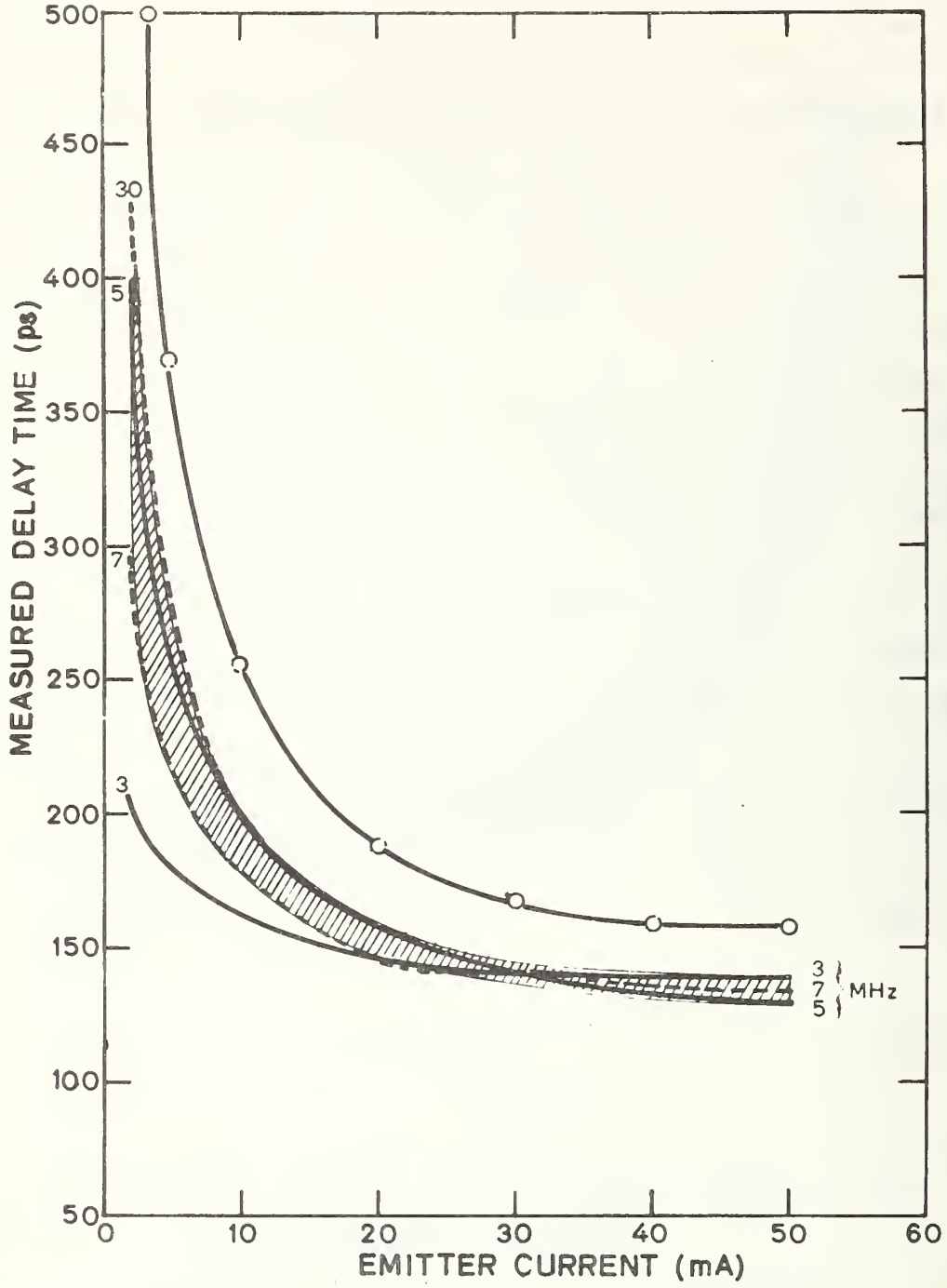

Figure 17. Results of Interlaboratory Comparisons Of Delay Time Measurements Made With Two Sandia Briges On a Second Special High-frequency Transistor. The NBS Values Measured Between 7 And 30 MHz Lie Within The Cross-hatched Area. The NBS Measurements Were Made at Frequencies Between 3 And 30 MHz, While Measurements Made At The Other Laboratory, Shown With Circles, Were Made At 10 MHz.

SECTION III

PROBE AC MEASUREMENTS OF INTEGRATED CIRCUITS AT THE WAFER LEVEL

1. INTRODUCTION

One might believe that the simplest means of testing transistors at the wafer level would be to use manually placed probes to make electrical contact to the transistor electrodes; indeed several authors have described techniques for measuring the high-frequency properties of devices and circuits in this way (references 5 and 6). A higher level of sophistication would be the use of a high-frequency probe assembly in an automatic prober; this procedure is a step beyond the current state of the art and is now under investigation by AFWL for acquiring S-parameter data on transistors embedded in special IC wafers.

Although the responsibility for the design of the IC wafers, with attendant acquisition and tests and the specification, acquisition and evaluation of the special high-frequency probes lay with AFWL, NBS provided assistance to AFWL in the

(a) specification of the IC wafers,
(b) characterization of the mechanical attributes of the special probes,
(c) characterization of the electrical attributes of the special probes, and
(d) characterization of the probe-IC wafer contact.

2. A PRECAUTION: EFFECTS OF PRESSURE ON DEVICE CHARACTERISTICS

Investigators have found that values of device characteristics measured when pressure is applied to the active region can differ greatly from those

that are measured otherwise. The word "active" refers, in this context, to *pn* junctions. The parameter value changes may be quite large but are reversible except when the elastic limit of the semiconductor is exceeded. For example, one investigator (reference 7) found that the common-emitter current gain of a transistor could be varied from 150 to 5 and back again as pressure was applied and released. Theory and experiment (reference 8) show that large changes in current gain can be explained by considering the effects of pressure on the band structure of the semiconductor, and that modern high-frequency transistors, which have shallow emitter-base junctions, are particularly susceptible to pressure effects. The stress sensitivity of transistors (reference 9) and diodes (reference 10) has been employed as the operating mechanism of devices intended to be practical pressure transducers. It is noteworthy that the effects on diode parameters may also be large. Reversible changes by a factor of four in emitter-base capacitance have been reported (reference 7). Significant changes in diode forward current-voltage characteristics and drastic changes in diode reverse-bias breakdown voltage have also been observed (reference 10). For a program involving the automatic probing of devices at the wafer level, it is essential, therefore, that connections to device active regions be brought out to pads. Another consideration particularly with an automatic probing system is that the probe force may be large enough to puncture the transistor emitter and thus permanently degrade the emitter-base junction. This is particularly likely to occur if the probe tips are sharp, if they slide after making contact, or both. Based on this information, specifications on the locations of the test and bonding pads were subsequently changed so that contact pads no longer were planned to be above transistor active regions.

3. DESCRIPTION OF AFWL SPECIAL TRANSISTOR PROBE ASSEMBLIES

The design of the special IC wafers to be probed and the design of the high-frequency probe assemblies must of necessity be interdependent. The AFWL determined a compatible set of IC wafer and probe assembly designs and ordered a set of six probe-assemblies. The assemblies were designed to contact

square in-line transistor pads 0.002 in. (50.8μm) on a side and 0.003 in. (76.2μm) between centers. Of the six probe assemblies, three have the common (or circuit return) probe in the center, and three have the common probe at one end. A photograph of the tip portion of one of the former is shown in figure 18. The gold-plated, beryllium-copper probes are bonded to the perimeter of a 2.5 mm-diameter hole in a sapphire plate approximately 0.65-mm thick. The beryllium-copper pieces are bent 90 deg around the hole rim and end about 0.3 mm below the surface of the sapphire as in-line tips spaced about 0.003 in. (76.2 μm) between centers. The construction allows one to determine, by looking through the hole in the sapphire plate, which portions of the bonding pads are contacted by the probe tips. The sapphire plate also serves as the dielectric of 50-Ω strip transmission lines made by depositing two metal-film stripes on the sapphire, one connected to each of the two above-ground probes. Each stripe is flanked by deposited metal films connected to the common probe. The probe and strip-line assembly is protected by mounting the sapphire plate in a sturdy, rectangular brass case, open in the center. The case also serves as the mount for two 50-Ω miniature coaxial connectors connected to the ends of the metal-film strips remote from the probe tips.

4. CHARACTERIZATION OF AFWL SPECIAL TRANSISTOR PROBE ASSEMBLIES

Probe assembly characterization has ranged from measurements yielding practical mechanical information designed to assist in adjusting the automatic prober for reliable contact between the probe tips and transistor contact pads, to equally practical work calculating the contribution of the probe assembly itself to transistor S-parameter values obtained using the probes.

a. Mechanical Characterization

The highlights of the results of measurements of the mechanical attributes of the AFWL special probes are presented in this section.* Most of the meas-

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* Quantitative data on the individual probe assemblies were reported to the AFWL in a letter report.

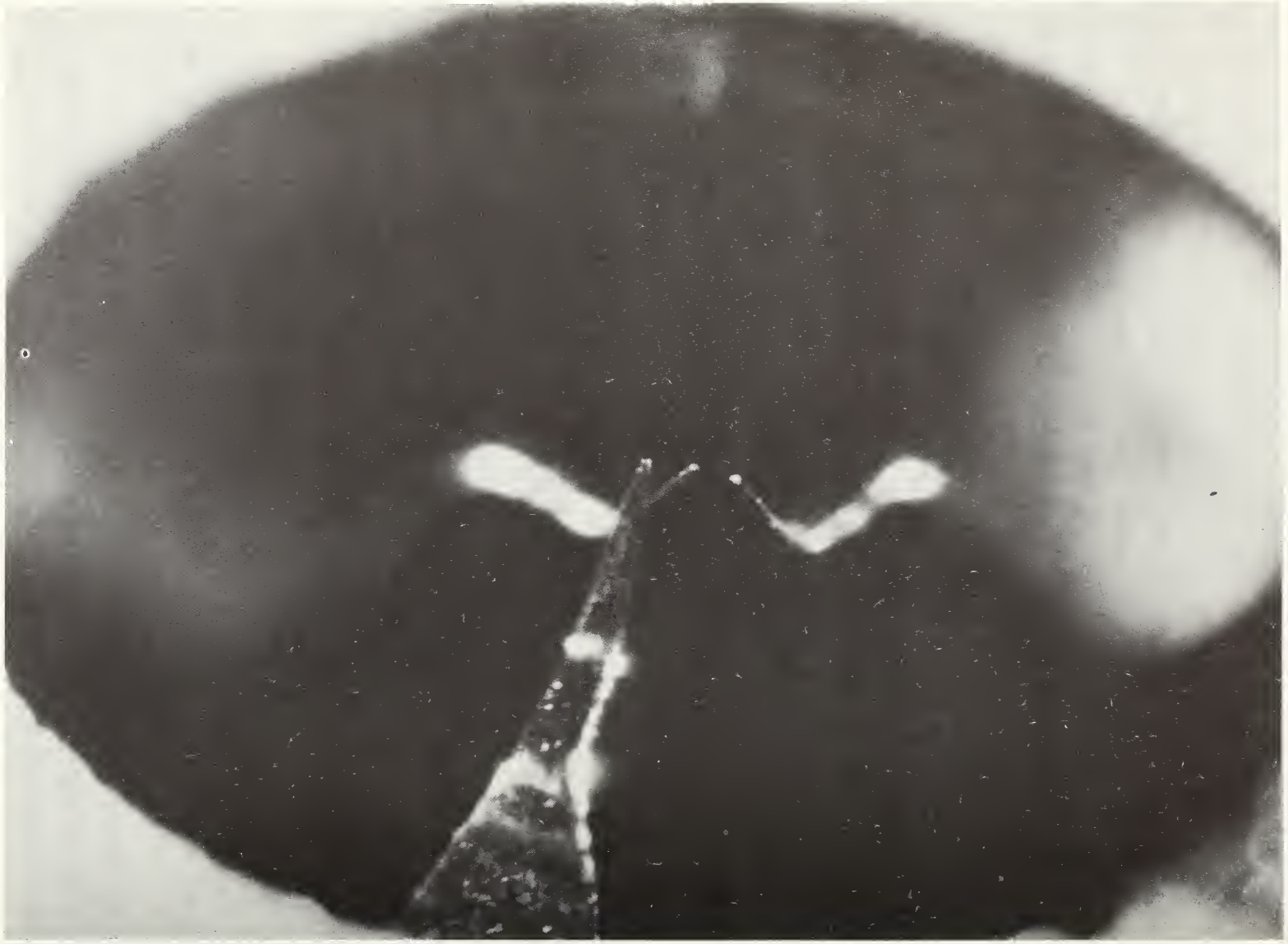

Figure 18. Photograph of a Special Probe Assembly (64 x Magnification)

urements were performed using an apparatus which was designed by NBS originally for measuring probe loading of four-point probes used for semiconductor resistivity determination (Reference 11). The apparatus was modified for the present service by adding an appropriate fixture to hold the probe assemblies (figure 19).

Optical measurements were first made of the relative protrusion of the probe tips, with the tips uncontacted. Next, probe restoring force measurements were made by pressing the probe tips, singly and in combination, against the gold-plated, stainless steel anvil in the apparatus shown in figure 19 and recording the force for a depression of the probe points 1.5 mils (38 μm) from the reference established by the rest position of the longest probe point.

Probe tracks were also recorded using the same apparatus. The probe tips were pressed with various forces against aluminized silicon wafers cemented to the anvil. Microscope examination of the wafer surfaces then yielded the degree and the direction of probe skid for each probe point. The test specimens were prepared in a manner typical of that used for the preparation of IC contact pads: Aluminum was evaporated to a thickness of about 8,000 Angstroms (0.8 μm) on approximately 5,000 Angstroms (0.5 μm) of silicon dioxide on silicon. The samples were heated to about 550°C after aluminum deposition. One conclusion reached after examining the probe tracks is that probe-contact pad resistance is not expected to affect the results when IC transistors are measured: inspection of the skid marks left on the test specimens suggests that insulating films such as thin native oxides between the probe metal and the pad metal would be ruptured mechanically (reference 12). This is fortunate since an intact oxide film sandwiched between a probe tip and a pad could yield an erratic and uncontrollable resistance.

Photomicrographs of the probe tips at magnifications up to 1240 X were made following these measurements. Comparisons with similar photomicrographs made before beginning showed no discernable changes, and so these measurements caused no damage to the probe assemblies.

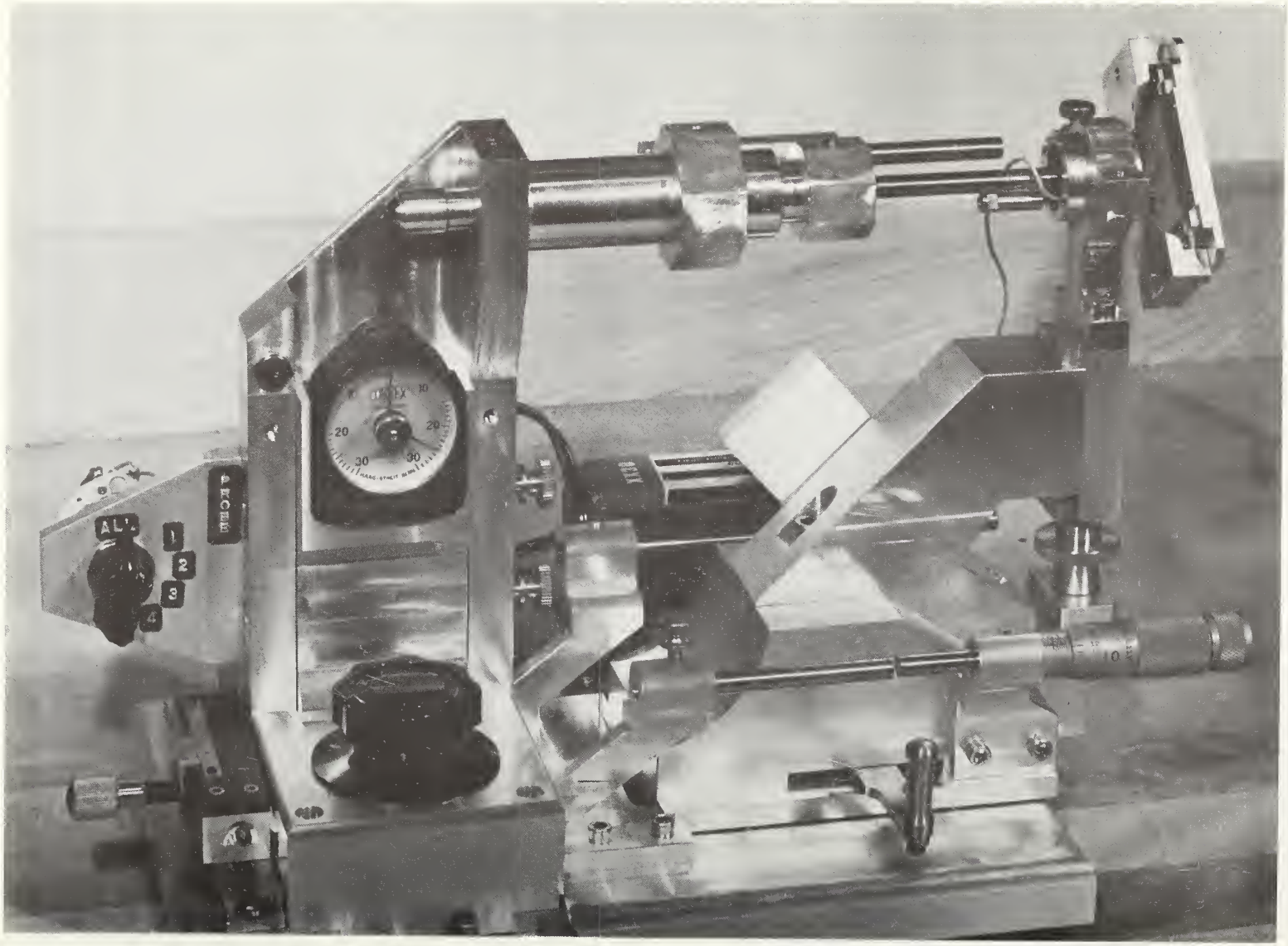

Figure 19. Apparatus Used for the Measurement of Probe Restoring Force and for the Recording of Probe Tracks on Aluminized Silicon Wafers.

b. Electrical Characterization

In order to determine and correct for the effects of the probe assemblies themselves on the measurements, it is necessary to determine experimentally the element values in the equivalent circuit representing the assemblies. The network between a connector port and the associated probe tip set (one tip at ground potential and the other above ground) making up one-half of a probe assembly can be represented by a pi equivalent circuit of three impedances. Complete electrical characterization of the network is achieved when these impedances are determined. Their values at a given frequency can be found using the analysis developed in Appendix III and the techniques outlined therein. One makes measurements at the connector ports with the probe tips in contact with elements having known impedance values. Since the network is represented by three (initially unknown) elements, three different probe tip terminations are required. In effect, the sequence of measurements yields three equations in the three probe-impedance unknowns, and so the unknowns may be determined simultaneously. The electrical terminations, also known as probe reference units, chosen are an open circuit, a short circuit, and a resistor of known value.

The probe reference units (PRUs) were fabricated on alumina substrates, 1 in. (25 mm) square by 0.015 in. (0.38 mm) thick, by a sequence of masking and etching operations. As received the substrates were coated with 6.3 μm of gold over 10 nm of chrome over tantalum nitride with nominal sheet resistivity of 40 Ω/□. A typical finished unit is shown in figure 20. The white background material is the bare ceramic substrate, the gray areas are the gold contact pads, and the dark regions are the exposed tantulum nitride. The narrow contact stripes are 0.002 in. (0.05 mm) wide and 0.006 in. (0.15 mm) long. The U-shaped structure at the center of the unit enables the resistance between the contact pads and the resistive film to be determined.

There are about 400 such units on each PRU wafer. The open circuits and short circuits of the PRUs may be considered as interchangeable, one with another, but it is not wise to assume that any of the resistive elements

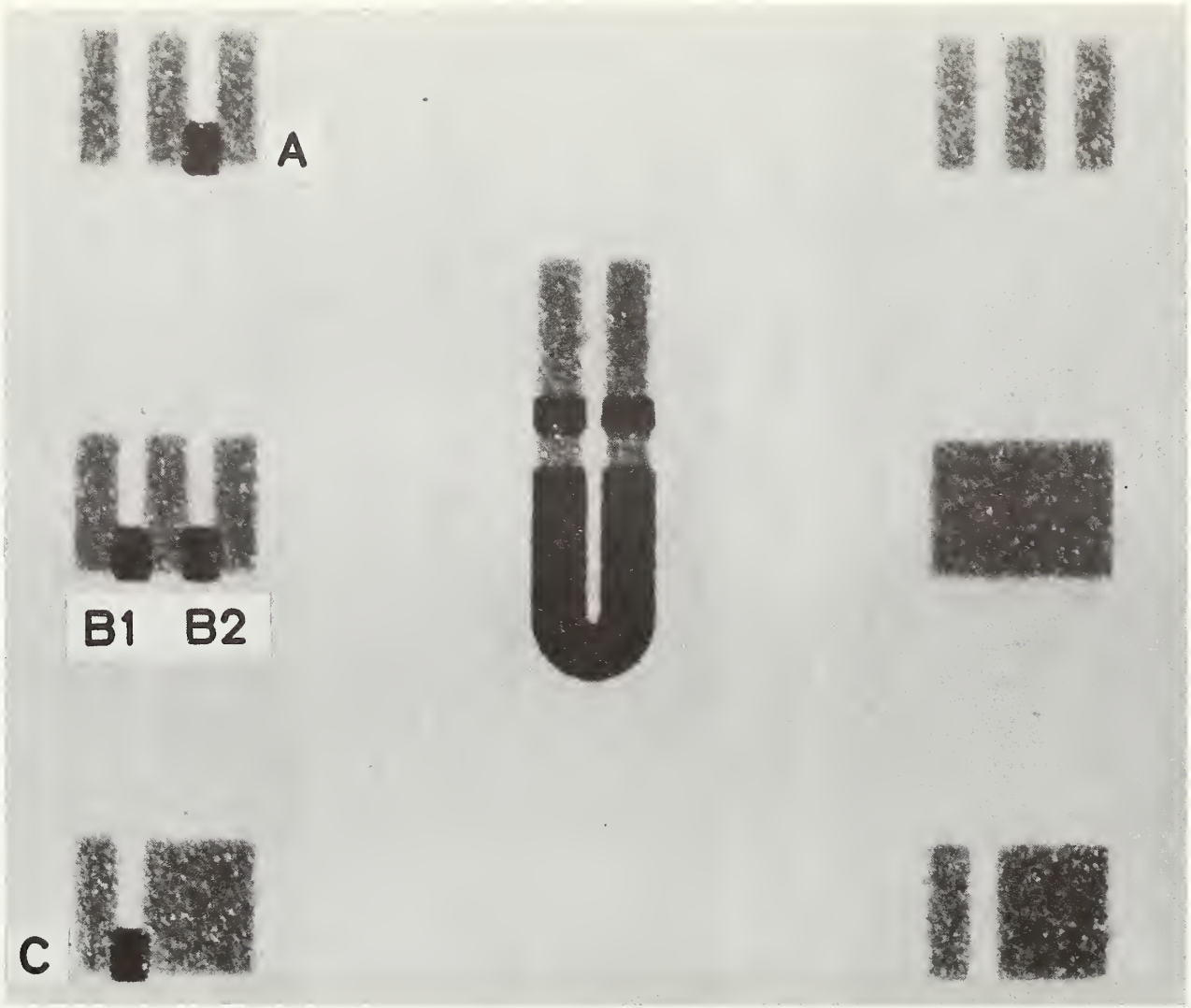

Figure 20. One Array of PRUs. The Central U is a Special Pattern for Determining the Characteristics of the Multi-Layered Metal and Nitride Films as Deposited. The Elements to the Right are Various Short Circuit and Open Circuit Combinations, While Those to the Left are Various Combinations of Resistors, Short Circuits and Open Circuits.

of a given type on a given wafer are similar. The resistance may vary from unit to unit due to unavoidable variations in the sheet resistance of the tantalum nitride layer, in the alignment and tolerances of the fabrication masks, and in the action of the chemical etches used in fabricating the resistive elements. A scheme to uniquely describe the location of any particular resistive element in the wafer was developed. The locating scheme is illustrated with the aid of the photograph of a portion of a PRU wafer, shown in figure 21. The "U" of a unit close to the center of the wafer is marked with a dot of dye to define the origin of coordinates, and the convention is established that the wafer is always described as if it were placed with the "U"'s opening away from the observer along the y-axis. Any "U" in the wafer may be located relative to the dye-marked one by knowing its x and y coordinates. For example, the "U" second to the right of the dye-marked one and in the first row below would be designated (2, -1). Within a particular unit, the resistors are identified by letter symbols as shown on the left-hand side of figure 20.

Designated resistive elements in probe reference unit number six were measured and the values recorded as shown in Table III. These resistors can be shown to have values which are, to all practical purposes, independent of frequency to beyond 2 GHz, the upper limit of the transistor-measurement equipment. The resistors were measured by d-c potentiometric (Kelvin) methods. Figure 22 is the photograph of a work station assembled for this purpose. It is equipped with a microscope to allow PRU wafers to be translated and rotated in the horizontal plane and raised and lowered in the vertical plane. This allows any PRU resistive element to be measured by bringing it into contact with a set of four electrolytically sharpened probes which are connected to a standard four-probe electrical circuit (reference 13).

An entirely separate work station, with features similar to the one described above was assembled for use in obtaining the data necessary to characterize the high-frequency properties of the probe assemblies and is shown in figure 23. In this work station, a probe assembly and a PRU wafer

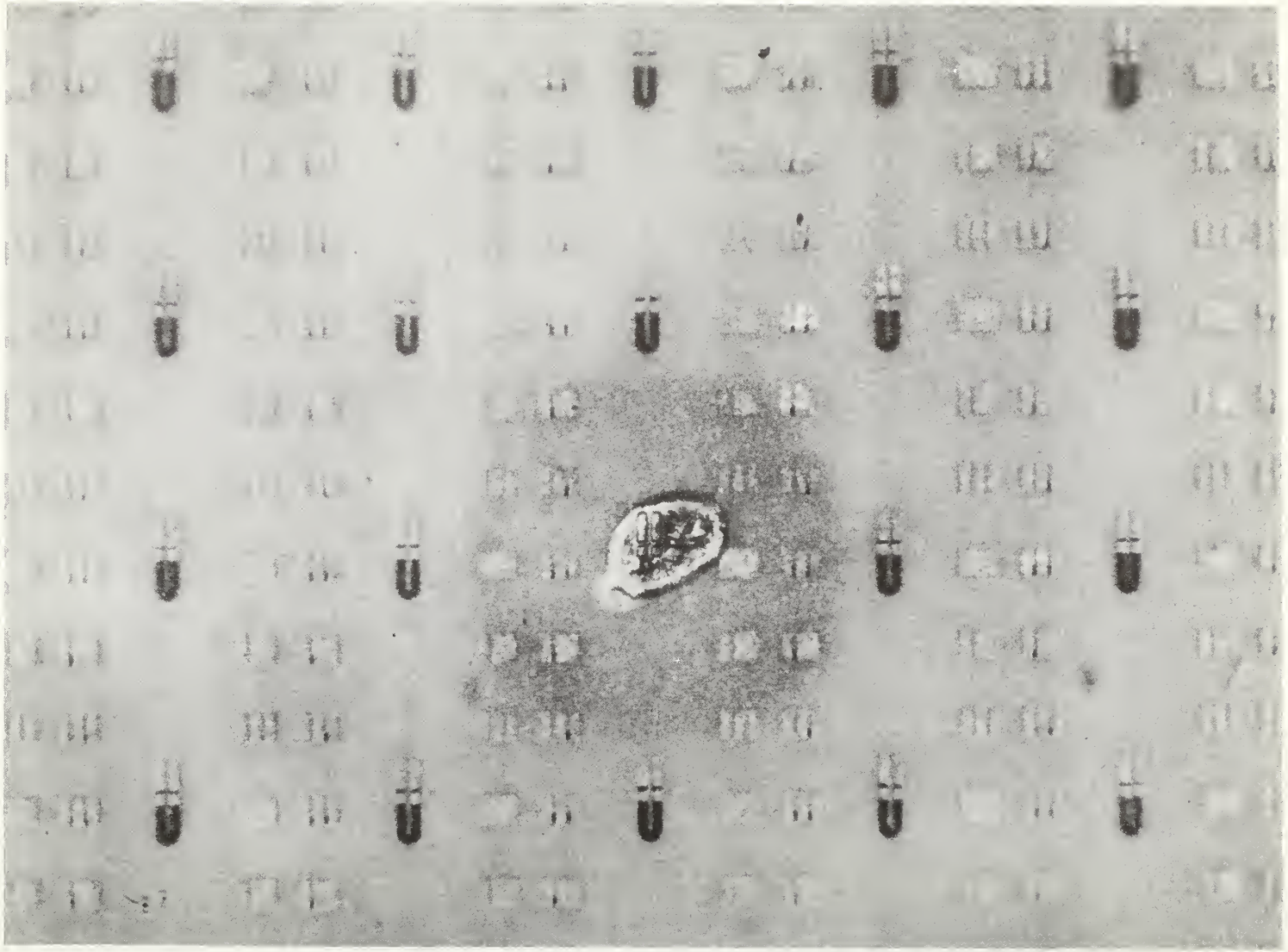

Figure 21. A Photomicrograph of a Portion of a PRU Wafer. The ∪ marked With Dye Established the Origin of the Coordinate System Used to Locate any Resistive Element on the Wafer.

TABLE III

The Electrical Resistance of Designated Elements
in Probe Reference Unit Wafer No. 6

UNIT	RESISTANCE OF DESIGNATED ELEMENT (Ω) A	B1	B2	C
First Quadrant				
(1, 3)	20.6	22.6	21.6	24.6
(2, 0)	22.5	22.7	22.1	24.2
(2, 1)	25.8	21.6	23.8	24.1
(2, 2)	23.1	22.4	22.9	24.0
(2, 3)	21.9	24.0	23.5	24.3
Second Quadrant				
(-2, 3)	20.41	22.43	20.77	22.47
(-3, 0)	20.85	21.76	22.19	22.17
(-3, 1)	20.98	21.44	21.95	24.44
(-3, 2)	22.68	23.86	22.78	23.55
(-3, 3)	22.77	26.01	25.69	26.33
Third Quadrant				
(-2, -3)	20.50	21.80	19.63	21.46
(-3, -1)	22.60	22.56	21.13	23.11
(-3, -2)	20.53	20.30	19.06	20.64
(-3, -3)	20.18	21.10	19.80	20.95
Fourth Quadrant				
(0, -3)	-----	20.98	19.18	21.08
(1, -3)	21.11	21.62	19.60	19.70
(2, -1)	21.60	24.80	23.10	18.70
(2, -2)	22.80	21.40	21.40	19.50
(2, -3)	25.00	21.80	21.70	23.40

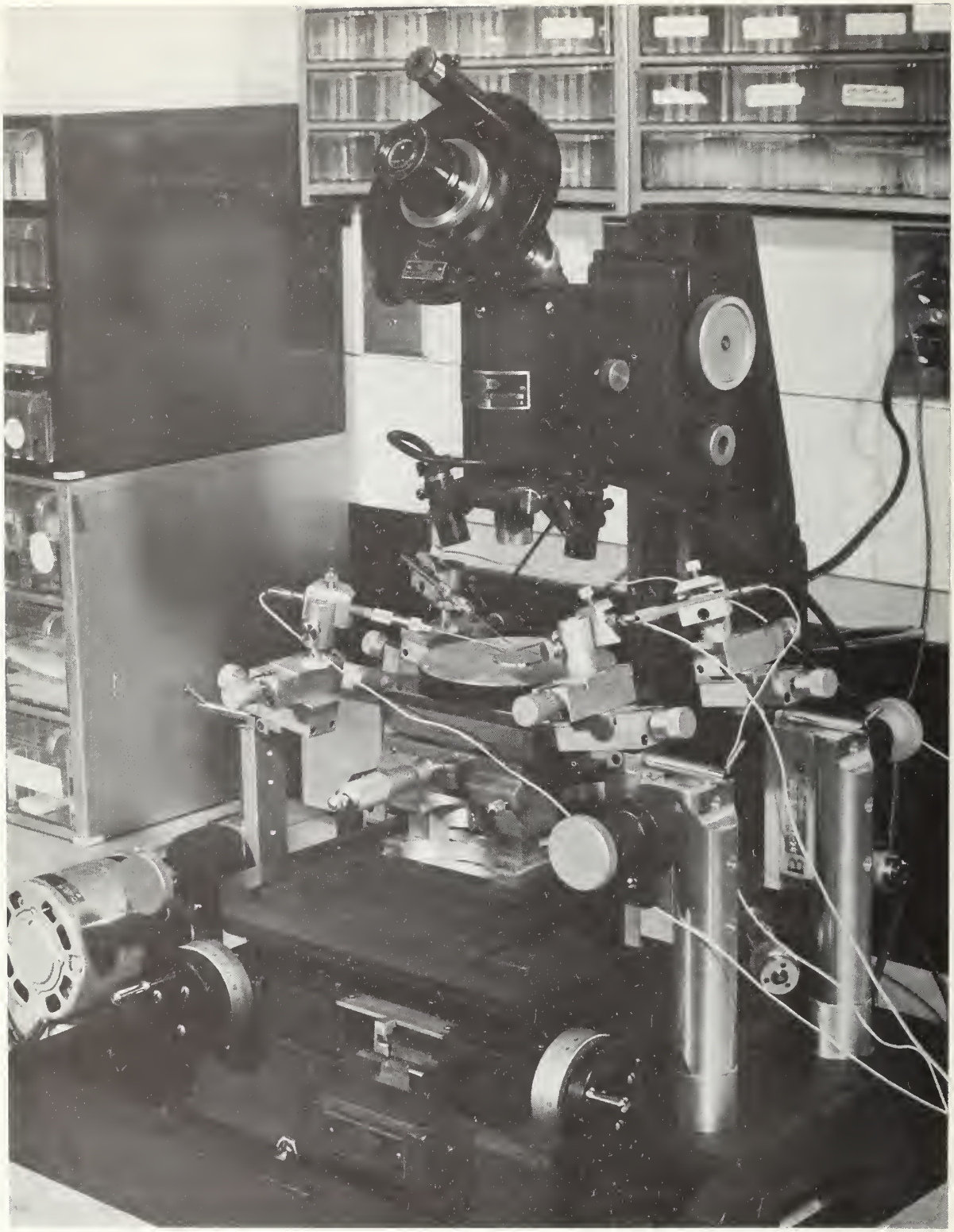

Figure 22. The Work Station Used to Measure the Resistance of the Resistors in the PRU.

Figure 23. The Work Station Used to Move a Probe Assembly and a PRU Wafer Relative to Each Other.

can be moved relative to each other, and a known termination such as a short, open, or resistance can be placed across the appropriate probe tips. Characterization of the probe assemblies using the equipment and techniques described is in progress.

SECTION IV

S-PARAMETER MEASUREMENTS

1. GENERAL

For small-signal ac analysis it is common practice to consider the transistor as a four-terminal network with the voltages and currents at the input and output terminals related by a set of four parameters. The most common sets employed are the h, y, and z-parameters. The measurement of any of these sets of parameters requires that measurements be made with input and output of the device open circuited or short circuited (reference 14). This is difficult to do at high frequencies, typically requiring a separate adjustment of tuning stubs for each frequency. Furthermore, stable transistor operation may be difficult to achieve at high frequencies with a short circuit at the input or output.

At frequencies in the VHF and UHF regions, it is more convenient to measure transistors in a circuit which is terminated in its characteristic impedance, thus eliminating the instability problem and the necessity for tuning adjustments at each frequency. In this case, the parameters used to define the transistor relate the waves reflected from the device to those incident upon it, and are called the scattering, or S, parameters. In figure 24, a_1 and a_2 represent incident waves at the input and output terminals, respectively, while b_1 and b_2 represent reflected waves. The wave leaving the input terminal, b_1, is a function of both the portion of the incident wave that is reflected from the input terminals and the portion of the wave incident on the output terminals that is transmitted through the device. Similarly, the wave leaving the output terminals is a function of the waves incident on both the input and output terminals. These waves are related by the equations

$$b_1 = s_{11}a_1 + s_{12}a_2 \tag{18}$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

The constants which relate the incident and reflected waves, s_{11}, s_{22}, s_{21}, s_{12}, are scattering parameters. They are frequency-dependent, dimensionless, complex numbers.

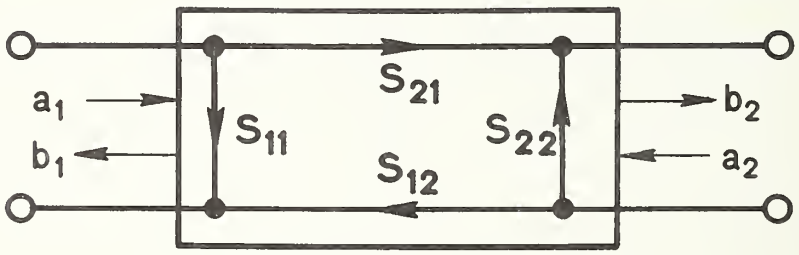

Figure 24. Four-Terminal Network Characterized by S-Parameters.

To measure or define the scattering parameters, the transistor is terminated at both input and output by a pure resistance, Z_o, which is equal to the characteristic impedance of the connecting line (figure 25). Under these conditions, no signal is reflected from source or load. With source and load connected as shown in figure 25, $a_2 = 0$, and the defining equations may be solved for s_{11} and s_{21}.

$$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} \tag{20}$$

$$s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} \tag{21}$$

If the generator and load in figure 25 are interchanged, a_1 becomes zero and the equations can be solved for s_{12} and s_{22}.

$$s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0} \tag{22}$$

$$s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} \tag{23}$$

Most measurements are made with Z_o equal to 50 Ω.

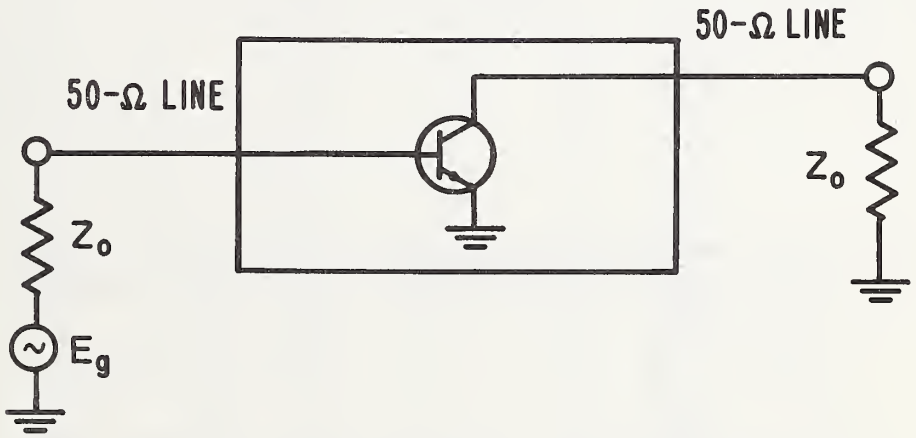

Figure 25. Circuit for the Measurement of S-Parameters.

The incident and reflected waves used to define the scattering parameters are related to the terminal currents and voltages used to define the h, y, and z-parameters, figure 26, by the equations (reference 14)

$$V_1 = a_1 + b_1 \tag{24}$$

$$V_2 = a_2 + b_2 \tag{25}$$

$$I_1 = \frac{a_1 - b_1}{Z_o} \tag{26}$$

$$I_2 = \frac{a_2 - b_2}{Z_o} \tag{27}$$

where a_n and b_n (n = 1 or 2) are the incident and reflected waves defined in figure 24, V_n and I_n are the corresponding values of voltage and current defined in figure 26, and the impedances at the terminals in either case are equal to Z_o. All of these are usually complex quantities. These relationships permit S-parameters to be mathematically transformed to h, y, or z-parameters, and vice versa, as summarized in Table IV.

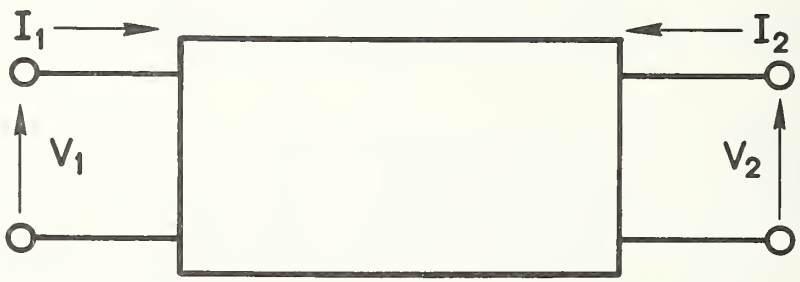

Figure 26. Terminal Voltages and Currents Defined for y-, z-, h-Parameters.

The subscripts used in defining the S-parameters and in Table IV are general and apply to any network. The first number in the subscript indicates the terminal at which the dependent variable is to be read with respect to the independent variable at the terminal indicated by the second number.

Table IV

Conversion Equations Between

Z, Y, H and S-Parameters

Part 1. S to Z and Z to S Conversions

$$S_{11} = \frac{(Z_{11} - 1)(Z_{22} + 1) - Z_{12} Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12} Z_{21}} \qquad Z_{11} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12} S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12} S_{21}}$$

$$S_{12} = \frac{2Z_{12}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12} Z_{21}} \qquad Z_{12} = \frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12} S_{21}}$$

$$S_{21} = \frac{2Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12} Z_{21}} \qquad Z_{21} = \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12} S_{21}}$$

$$S_{22} = \frac{(Z_{11} + 1)(Z_{22} - 1) - Z_{12} Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12} Z_{21}} \qquad Z_{22} = \frac{(1 + S_{22})(1 - S_{11}) + S_{12} S_{21}}{(1 - S_{11}) - (1 - S_{22}) - S_{12} S_{21}}$$

Table IV

Conversion Equations Between

Z, Y, H and S-Parameters

Part 2. S to Y and Y to S Conversions

$$S_{11} = \frac{(1 - Y_{11})(1 + Y_{22}) + Y_{12} Y_{21}}{(1 + Y_{11})(1 + Y_{22}) - Y_{12} Y_{21}} \qquad Y_{11} = \frac{(1 + S_{22})(1 - S_{11}) + S_{12} S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12} S_{21}}$$

$$S_{12} = \frac{-2Y_{12}}{(1 + Y_{11})(1 + Y_{22}) - Y_{12} Y_{21}} \qquad Y_{12} = \frac{-2S_{12}}{(1 + s_{11})(1 + S_{22}) - S_{12} S_{21}}$$

$$S_{21} = \frac{-2Y_{21}}{(1 + Y_{11})(1 + Y_{22}) - Y_{12} Y_{21}} \qquad Y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12} S_{21}}$$

$$S_{22} = \frac{(1 + Y_{11})(1 - Y_{22}) + Y_{21} Y_{12}}{(1 + Y_{11})(1 + Y_{22}) - Y_{12} Y_{21}} \qquad Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12} S_{21}}{(1 + S_{11})(1 + S_{11}) - S_{12} S_{21}}$$

Table IV

Conversion Equations Between

Z, Y, H and S-Parameters

Part 3. S to H and H to S Conversions

$$S_{11} = \frac{(h_{11} - 1)(h_{22} + 1) - h_{12} h_{21}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}} \qquad h_{11} = \frac{(1 + S_{11})(1 + S_{22}) - S_{12} S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}}$$

$$S_{12} = \frac{2h_{12}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}} \qquad h_{12} = \frac{2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}}$$

$$S_{21} = \frac{-2h_{21}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}} \qquad h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}}$$

$$S_{22} = \frac{(1 + h_{11})(1 - h_{22}) + h_{12} h_{21}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}} \qquad h_{22} = \frac{(1 - S_{22})(1 - S_{11}) - S_{12} S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}}$$

Thus, s_{21}, designates the portion of the signal emerging from terminal 2 which is the result of the signal incident on terminal 1, and h_{21} relates the current at terminal 2 to the current at terminal 1.

A different notation is often used with transistors. In this notation, the first character indicates the terminals at which the measurement is made using i for input o for output, f for forward (output terminal with respect to input), or r for reverse (input terminal with respect to output). The second character in the subscript indicates the transistor terminal that is common to both input and output circuits by e, b or c for common emitter, base or collector. Thus, s_{21} could be written as s_{fe} if the transistor is connected in the common emitter configuration, and h_{21} becomes h_{fe}.

2. TRANSIT TIME MEASUREMENTS

Transistor scattering parameters have been used as an independent method of determining base transit time for comparsion with the results of transit time measurements made on the Sandia bridge and vector voltmeter. The S-parameters are used to determine common emitter current gain h_{fe}, as a function of frequency and emitter current, from which the transition frequency, f_T, and total delay time, τ_T, can be determined (reference 16).

The method is illustrated by the measurements on a 2N2219 *npn* silicon transistor whose transit time had previously been determined as described in Section II. Amplitude and phase of the four S-parameters were measured over a range of emitter biases and at several frequencies in the region in which h_{fe} varies inversely with frequency. From these data, h_{fe} was calculated from the equation for h_{21} in Table IV. Transition frequency, f_T, was determined by plotting h_{fe} in decibels against log frequency and extrapolating to the unity gain intercept on the frequency axis, as shown in figure 27. Total delay time, $\tau_T = 1/(2\pi f_T)$, was then calculated for each value of emitter current and plotted against the reciprocal of emitter current as illustrated in figure 28. The straight line portion of the curve was extended to the total delay time axis to determine the time extrapolated to infinite emitter current or the base transit time. The value so obtained agrees within about 5% with that obtained from measurements made with the vector voltmeter system at large emitter currents (figure 15).

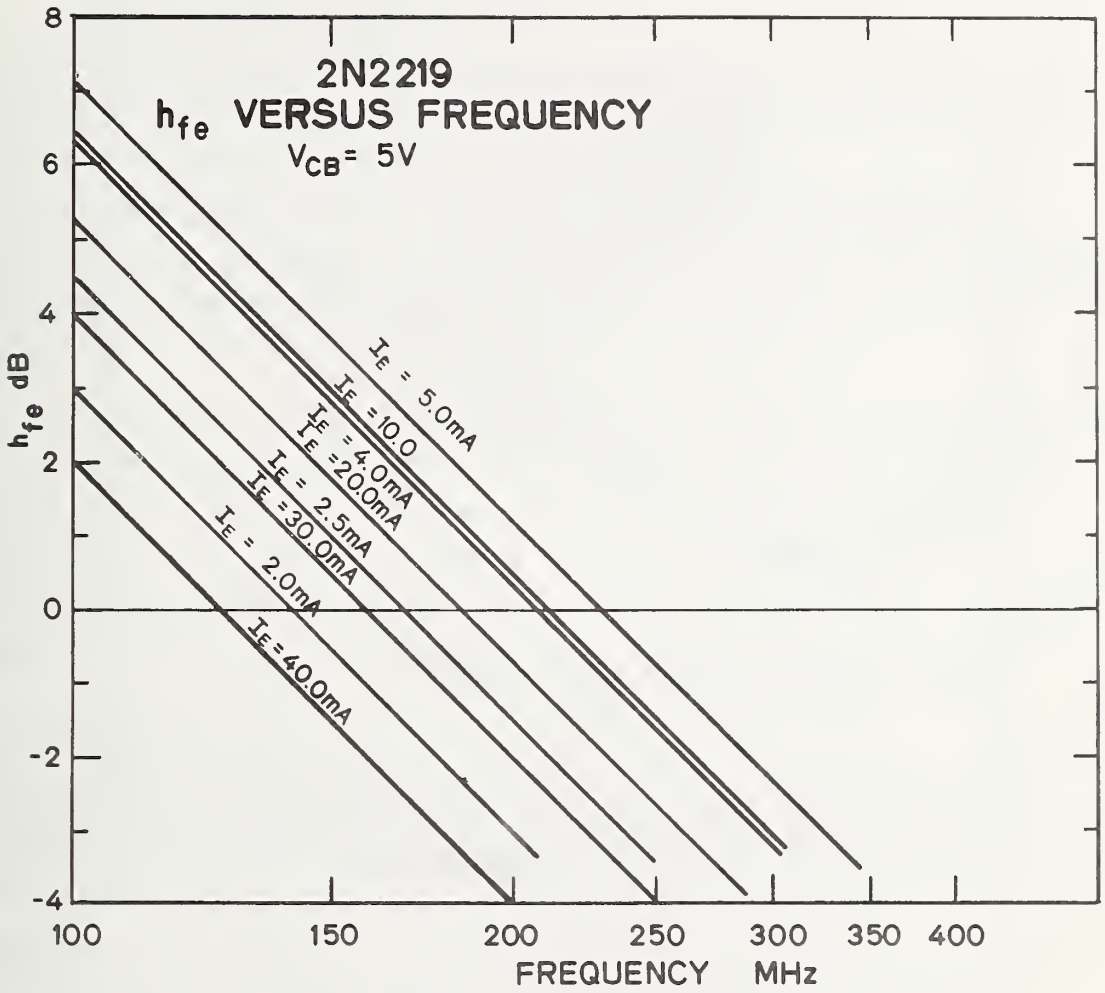

Figure 27. Variation of Small-Signal Forward Current Gain With Frequency for a 2N2219 Transistor.

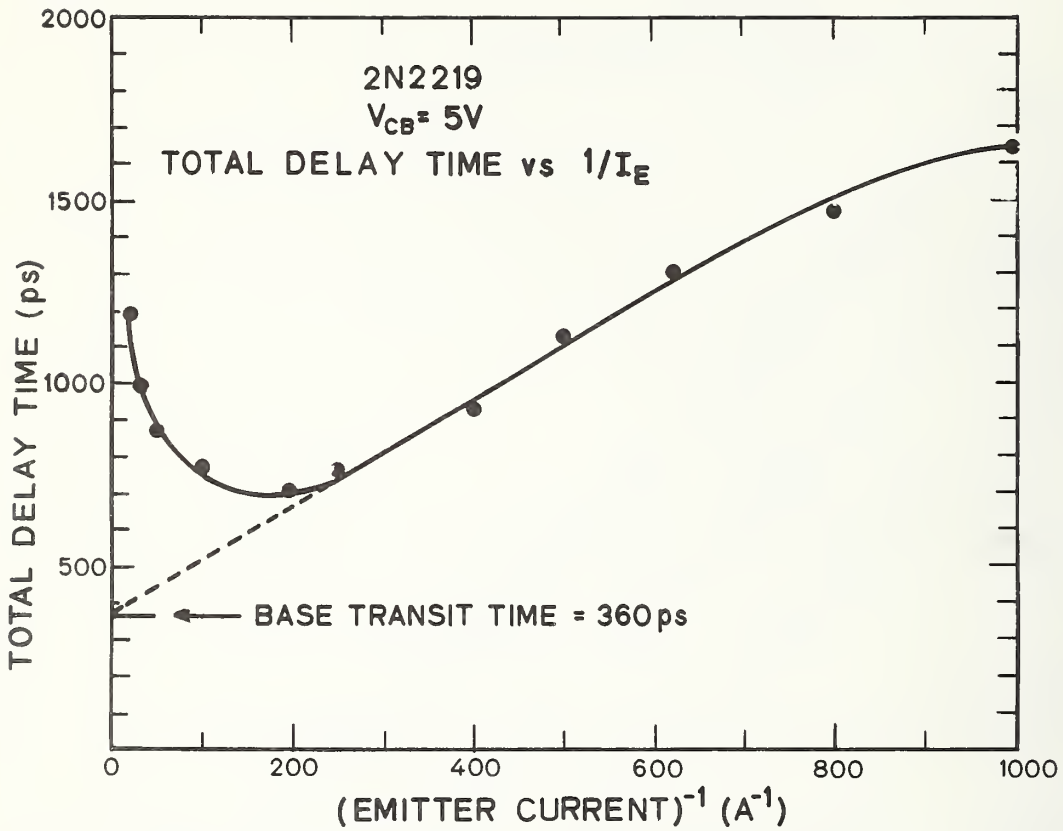

Figure 28. Total Delay Time for a 2N2219 Transistor as a Function of the Reciprocal of Emitter Current.

3. INTERLABORATORY COMPARISON OF TRANSISTOR S-PARAMETER MEASUREMENTS

In a recent study* of the state of the art of scattering parameter measurements over the frequency range between 100 MHz and 12 GHz it was reported that the resolution of typical equipment and techniques used in the measurement of reflection coefficients is 0.01. The magnitude of the phase angle error, in degrees, is approximately equal to the reciprocal of the reflection coefficient. Using the best equipment and techniques, resolution can be improved to 0.001, and the magnitude of the error in phase measurement, expressed in degrees, reduced to approximately one-tenth the reciprocal of the reflection coefficient (reference 16).

The accuracy of gain or attenuation measurements is the same for either of the methods mentioned above. If the gain or attenuation is 12 dB or greater, the error in decibels is 1% of the magnitude of the gain or attenuation in decibels. Between 0 and 11-dB gain or attenuation, the error increases from 0.1 dB to 0.12 dB. The phase angle can be measured within 1 deg if gain or attenuation is 25 dB or less. For a gain or

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* The material in the first two paragraphs of this section is taken from a paper prepared by R.C. Powell for the Task Group on Transistor Scattering Parameter Measurement Standards of JEDEC Committee JC-24 (formerly JS-9) on Low-Power Transistors. This report has since been incorporated as an appendix to the proposed Electronic Industries Association standard for the "Measurement of Small-Signal Transistor Scattering Parameters." The author, then with NBS, is now with the Office of Telecommunications, U.S. Department of Commerce. NBS maintains representation on the Task Group to provide contact with an industry group concerned with problems in the measurement of transistor scattering parameters.

attenuation between 25 and 50 dB, this error increases by about 0.15 deg/dB for each decibel in attenuation in excess of 25 dB.

A question of more practical interest to users of transistors is the extent to which S-parameter measurements agree when made on measuring equipment normally employed by users and suppliers. An interlaboratory comparison of transistor scattering parameter measurements was designed to determine the extent of the variability when devices are measured on different instruments in different locations. Seven organizations were contacted by AFWL and agreed to participate. In addition to the Boulder Laboratories of the National Bureau of Standards, these include one other government laboratory, three transistor suppliers, and two transistor users. All but one plan to make the measurements on an automatic network analyzer; the other will use the manually operated equivalent. Only one plans to set the transistor biases automatically.

A proposed plan for making the measurements necessary for the interlaboratory comparison was prepared and revised in accordance with suggestions from the participants to obtain the final plan, which is described in Appendix V and illustrated in figure 29. After consultation with the Air Force Weapons Laboratory, transistor types 2N709, 2N918 and 2N3960 were selected from those of most interest to AFWL because they are mechanically interchangeable in that all have either TO-18 or TO-72 bases. Six transistors of each type are to be measured by each participant.

Since transistor performance is a function of bias setting and temperature, it was decided to include among the test elements passive devices not subject to these variations. For this purpose, several R-C networks of the type illustrated in figure 9 and discussed in Section II 3were assembled on TO-72 headers. In addition, two coaxial attenuators were included among the devices to be tested. The 10-dB attenuators are being measured to obtain data for comparison of the measurement systems at the output ports of the network analyzer, independently of any transistor fixtures. Differences that occur among participants when the NBS transistor fixture is added and the R-C networks tested can be attributed to differences in calibration with

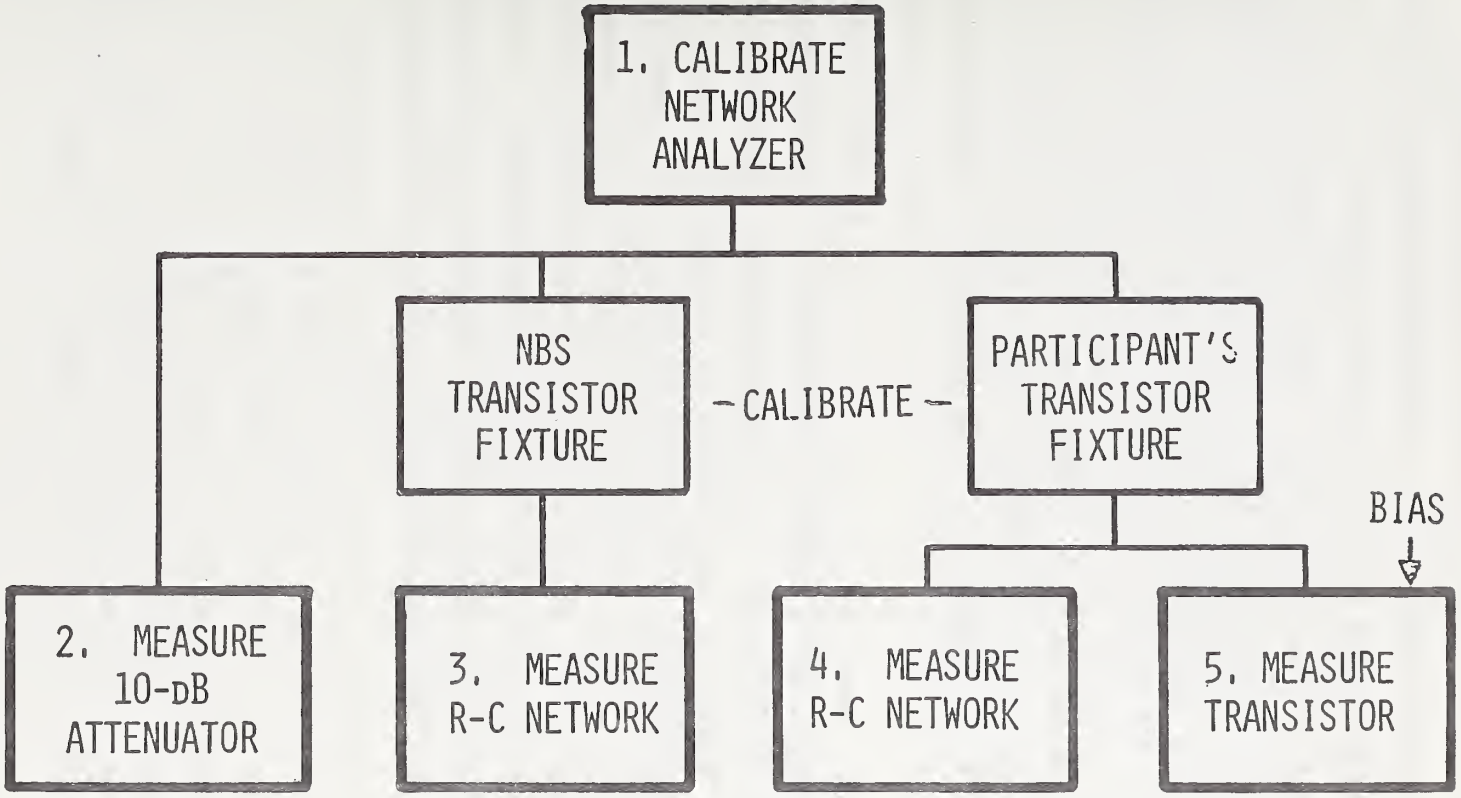

Figure 29. Test Plan for Interlaboratory Comparison of Transistor S-Parameter Measurements.

the transistor fixture in place, since all participants are to test the same devices using the same transistor fixture. The remaining measurements are made with the devices mounted in the participant's transistor fixture. The R-C networks are being measured in both transistor fixtures to disclose differences in the results caused by the transistor fixture.

Measurements similar to those described in Section IV 2 were made on typical transistors of the types to be used in the round robin to determine the frequency and emitter current range over which measurements are to be made. This resulted in the selection of 1.6, 2.0, 2.5, 4.0, 5.0, 8.0 and 10.0 ma for the emitter current, a collector to emitter voltage of 5 V, and a frequency range between 200 MHz and 1 GHz for the 2N709s and 2N918s and between 200 MHz and 1.8 GHz for the 2N3960s. These ranges were selected to permit use of the data to determine base transit time from calculated values of f_T.

Since changes in the transistor characteristics or inaccuracies in the bias settings would affect the S-parameter measurements, every effort has been made to minimize these errors. The transistors were either JAN-TX types, which had been "burned-in" for 168 h or were burned in under MIL spec conditions in our laboratory. Their characteristics were checked over a period of time and the most stable devices selected for the interlaboratory comparison. In addition, their S-parameters are to be recorded just prior to the beginning of the interlaboratory comparison, and measured on the same equipment several times during the round robin and compared with the initial measurements. Biases will be maintained within $\pm$ 0.1% for these measurements.

No accuracy was specified for the bias supplies to be used by the participants in the interlaboratory comparison, since the intent is to measure the transistors by the procedure normally employed. Most of the participants use a power supply with an accuracy of about $\pm$ 5%. No special provisions for the control of case temperature is proposed. A qualitative determination of the effect of case temperature on S-parameter measurements indicates that temperature effects are not a problem at the power levels used

in these tests provided the laboratory temperature is in the 20 to 25°C range. Since each of the participants will make four measurements on each passive device, a mean value and the standard deviation will be calculated to assess the variability of his measurements. These will then be compared with the over-all mean and standard deviation for all the participants to furnish each participant and AFWL with a measure of the quality of the measurements in relation to the average of all the others. The same procedure will be followed in the case of the transistor measurements except that each participant will measure the transistor only once at each bias, so there will be no averaging of each participant's data.

Several transistors and R-C networks have been measured as outlined in the round-robin plan at both the Boulder Laboratories of NBS and at the Sandia Laboratories. In addition, some of these devices have been measured on the manual S-parameter test set at NBS, Washington. The results are compared in Table V.

By delivering the devices to be measured to each of the participants in turn, NBS plans to have completed most of the data taking by late November. The participant using manual equipment will have completed his measurements during December, and one of the participants using automatic equipment will be scheduled after the beginning of the year at his request. If it is assumed that this schedule can be met, the variability of the measuring equipment will be determined by analysis of the data on the passive devices by the end of March, and the analysis of the transistor data will be completed and the final report on this work prepared by June 30, 1973.

Table V

Comparisons of S-parameter Measurements Made at Various Installations

	Number of pairs	Differences between pairs of measurements: Magnitude Mean	Magnitude Maximum	Magnitude No. greater than spec'd accuracy	Phase Mean	Phase Maximum	Phase No. greater than 4°
Transistor measurements[2]							
1. Boulder repeatability, h_{fe}	48	1.2%	2.3%	0			
Boulder repeatability, S21	48	1.1%	3.8%	0	0.5°	2.0°	0
2. Boulder - Sandia, h_{fe}	50	1.8%	7.0%	1			
Boulder - Sandia, S21	50	2.5%	14.5%	5	2.0°	5.0°	1
3. Washington - Boulder, h_{fe}	130	3.7%	25.2%	17			
Z parameters of RC networks[3]							
4. Boulder - Sandia, RC No. 1	36	4.8%	11.4%	14	4.3°	9.0°	18
Boulder - Sandia, RC No. 2	36	4.6%	10.8%	9	3.3°	9.0°	9
5. Washington - Boulder, RC No. 1[4]	24	8.4%	28.3%	13	6.1°	32.9°	13
Washington - Boulder, RC No. 2	24	3.3%	7.7%	2	1.7°	4.1°	2

[1] 5% for S21, 6% for h_{fe} or Z parameters. 4° is estimated accuracy for phase measurements.

[2] Differences expressed in percent of the mean of the two measurements.

[3] Differences expressed in percent of the mean of the Boulder and Sandia measurements.

[4] Large differences occur in the vicinity of a series resonant frequency.

SECTION V

CONCLUSIONS

1. TRANSISTOR DELAY TIME

Some of the causes of transistor transit measurement discrepancy have been disclosed and resolved during this investigation. Discrepancies between instruments of the same type may arise because of a lack of suitable instrument calibration, or because of extraneous pickup at the measurement frequency. For the two delay-time systems examined in detail, the Sandia bridge and the vector voltmeter apparatus, techniques were developed to check instrument calibration by checking the scale calibrations for the first, and the accuracy of the phase-angle presentation for the second. A generally applicable method of correcting for the effects of extraneous pickup was developed and applied to the NBS version of the Sandia bridge.

Measurements made using different types of instruments also may differ. Measurement discrepancy can occur for a very fundamental reason: the various instruments may be responsive to different combinations of the active and passive delay times within the network in the transistor socket. A comparison of the transistor delay time for the vector voltmeter system, equation 9, with that for the Sandia bridge, equation 10, illustrated this and showed that it is necessary to first analyze the entire measurement circuit, with the equivalent circuit of the transistor included, to establish the relationship between the indicated delay time and the delay time(s) of interest: those due to transit time, and those due to device R-C time constants. Only then can one state what is being measured.

A methodology which can be used to analyze any phase delay-time instrument was explicitly presented. The methodology was applied to the Sandia bridge and to the vector voltmeter system to yield the results mentioned; one also

can predict the effects of variations in transistor parameters such as h_{fe} on delay times obtained both for systems influenced by extraneous pickup and for systems not so influenced. For the former, anomalous values can be obtained after gain degradation such as may occur after neutron irradiation, but if the equivalent circuit of the transistor and the measurement circuit is known, the delay times may be corrected.

2. PROBE AC MEASUREMENTS OF ICs

The AFWL concept of combining probes with automatic equipment for measuring devices to determine, among other quantities, S-parameters from 200 MHz to 2.0 GHz, is a step beyond the current state of the art. NBS provided assistance on the use of probe assemblies purchased by AFWL. This was based partly on literature citations and partly on measurements performed at NBS. The citations clearly showed that surfaces directly above active device regions should not be probed since several of the most important transistor parameters including h_{fe} and junction breakdown voltage show large, but reversible changes with pressure.

Mechanical measurements were performed to obtain information necessary to adjust the automatic probing equipment when the probe assemblies are in place. One conclusion reached was that thin oxide films on the metallic IC pads should not cause a significant contact resistance; the slight sliding of the probe tips which occurs under normal conditions should be sufficient to disrupt any such film and allow the tips and pads to form low-resistance metal-to-metal contacts.

The techniques and equipment required to characterize the electrical effects of the probes on transistor measurements were developed and assembled. Arrays of reference units on ceramic wafers were fabricated to provide known terminations at the probe tips. With the tips so contacted, measurements at the RF ports yield admittance values of the elements in a pi equivalent-circuit representation of the probe assembly.

3. S-PARAMETER MEASUREMENTS

Transistor S-parameter measurements have been made as part of a program for developing an S-parameter round-robin. Six organizations have participated in the round-robin during the time of this reporting period. Transistors of various types, as well as R-C networks, coaxial attenuators, and a transistor test fixture, are being circulated. From results of measurements on these passive components measurement discrepancies, should they arise, can be pinpointed. The measurements will be made from 200 MHz to 2.0 GHz. From the S-parameter data to be furnished by the participants, NBS can also compute transistor parameters of interest to the radiation hardness community such as maximum available gain versus frequency, and transit-time, and so the round-robin data contains the kernels of useful intercomparisons other than just the S-parameters themselves.

SECTION VI

RECOMMENDATIONS FOR FURTHER WORK

1. MEASUREMENTS OF THE PARAMETERS OF DISCRETE DEVICES

The delay-time systems described in Section II employ low measurement frequencies. Delay times also may be obtained from S-parameter measurements, as was illustrated in the work reported in Section IV 3. An investigation into the use of S-parameters for measuring transistor quantities believed to be indicators of radiation hardness is a logical extension of the measurement work presented in Section II. An integral part of the investigation would be a comparison, if feasible, of these indicator quantities determined through S-parameter measurements with the same quantities obtained through the use of other techniques. Throughout the course of the work, the technical approach found very beneficial in the delay-time work (Section II) should be employed; that is, the equivalent circuit of the transistor should be explicitly included. For clarity, let us suppose that f_T is the device quantity that is to be investigated. In Section IV 3 it was shown how f_T values for a 2N2219 could be obtained from S-parameter measurements, although it is well known that transistor f_T values can be obtained from measurement schemes conceptually much simpler than those based on S-parameters. One such technique is described in reference 16. This technique is less expensive to implement than an S-parameter one; it would be useful to compare the measurement precision and general utility of the two.

In addition to determining the degree of agreement between values, say of f_T, obtained with instruments of different types, it is necessary for a serious investigation that the measured quantity be interpreted meaningfully. For example, some devices never show a 6-dB/octave slope in a plot of current

gain versus frequency. So, unlike the 2N2219 device whose charateristics are plotted in figure 26 and 27, they do not have an f_T value, if we accept the usual definition of f_T (reference 18). Other devices may exhibit a 6-dB/octave slope behavior over two or more unconnected frequency intervals, and so one obtains two or more f_T values when the 6-dB/octave slopes are extrapolated to unity gain. Still others show no relationship between the f_T value obtained from a 6-dB/octave extrapolation and the frequency at which the current gain actually is unity. Additionally, the current-gain plot may cross the unity gain line more than once. A fruitful area for continuing work would be an examination of the reasons why such varied forms of behavior are seen and the significance of this behavior to prediction of radiation effects. The use of other parameters to serve as an alternative to f_T, for radiation hardness assurance should be explored. One reason for this is that f_T measurements are sensitive to device parasitics, such as the base-collector capacitance, for example. Some other parameters, perhaps maximum available gain (reference 19), may be better behaved. Another possibility is S_{21}. That plots of S_{21} versus frequency are beginning to appear in manufacturers' literature indicates that the device and circuit designers already are interested in this for specifying devices. For whichever radiation hardness indicator that appears the most promising, a suitably designed and conducted round-robin should be conducted to ascertain the measurement reproducibility, and thus determine a good deal about its suitability as a workable radiation hardness screen.

2. AC MEASUREMENTS ON IC WAFERS

Probing techniques such as the ones described in Section III for determining the parameter values at the wafer stage of fabrication are beginning to attract serious attention from the device and circuit community. Other experimental probing techniques make use of an electron beam (reference 20) or a light beam (reference 21) as the source of injected current-carriers. With the appropriate terminals of the IC connected to an oscilloscope and

the oscilloscope beam and the beam incident on the IC deflected in synchronism, the oscilloscope presents a map of the IC's response to the exciting agent. The excitation can be modulated at a high frequency, even in the gigahertz range (reference 21), and so the oscilloscope can present a picture of the high-frequency behavior of the integrated circuit being scanned. Success in developing such non-contacting probing techniques would allow the achievement of many of the benefits sought through the mechanical probe work; such probing techniques might make unnecessary the special modification of the IC metallization required for the mechanical probing. Electron beam probes and perhaps optical ones can be extended beyond transistor characterization to the verification of the complete IC wafer. For example, it is possible to observe the progress of logic through a shift register which is pulse excited up to gigahertz repetition rates (reference 22).

APPENDIX I

VECTOR VOLTMETER DELAY TIME APPARATUS

1. TRANSISTOR ANALYSIS

a. Idealized Measurement Circuit

The vector voltmeter apparatus determines delay time by interpreting the phase shift between the collector and emitter currents in terms of delay time as given by equation 2a. For the transistor represented by figure 2 in the test setup of figures 3 and 4, the overall equivalent circuit of figure 30 is applicable, provided that the impedance between the collector and base transistor socket pins in zero; the purpose of C_{BC}, the 0.85 μF capacitor in figure 4, is to provide a low collector-base impedance.

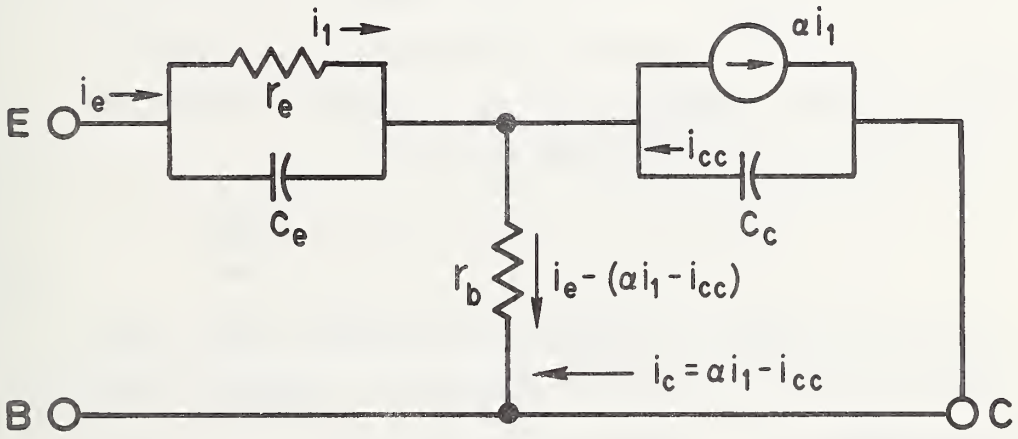

Figure 30. The Equivalent Circuit of an Idealized Vector Voltmeter Apparatus With the Transistor Represented by Figure 2 in the Transistor Socket.

The set of equations to be solved to relate the collector current to emitter current is

$$i_c = \alpha i_1 - i_{cc}$$

$$i_1 = \frac{i_e}{1+j\omega\tau_e} \tag{28}$$

$$\frac{i_{cc}}{j\omega\tau_{bc}} = \alpha i_1 - i_{cc} + i_e$$

and has the solution

$$\frac{i_c}{i_e} = \frac{\alpha+j\omega\tau_{bc}\ (1+j\omega\tau_e)}{(1+j\omega\tau_e)\ (1+j\omega\tau_{bc})} \tag{29}$$

We may write $\alpha = \alpha(\omega)e^{-j\omega\tau_\alpha}$ as before, and write $i_c/i_e = \eta(\omega)e^{-j\omega\tau}$ where τ_α and τ are real quantities. For $\omega\tau << 1$, the expansion of equation 29 accurate to the first power in ω is

$$\eta(\omega)[1-j\omega\tau] = \alpha(\omega)[1-j\omega(\tau_\alpha+\tau_e - \frac{\tau_{bc}}{h_{fe}})] \tag{30}$$

where we have made use of the definition of the small-signal common emitter current gain: $h_{fe} = \alpha/(1-\alpha)$. Equating the imaginary components of equation 30 yields

$$\tau = \tau_\alpha + \tau_e - \frac{\tau_{bc}}{h_{fe}} \tag{31}$$

b. Collector-Base Circuit Capacitive

If the collector-base loop is not a short-circuit, but rather is a capacitive reactance (due, e.g., to the use of a value for C_{BC} which is too small),

$$\frac{i_c}{i_e} = \frac{\alpha + j\omega\tau_{bc}(1+j\omega\tau_e)}{(1+j\omega\tau_e)[(1+\frac{C_c}{C_{BC}}) + j\omega\tau_{bc}]} \tag{32}$$

and so $$\tau = \tau_\alpha + \tau_e - \frac{\tau_{bc}}{h_{fe}} - \frac{\tau_{bc}}{\left(1+\frac{C_{BC}}{C_c}\right)}$$

The delay time is neglibibly different from the collector-base short-circuit case provided that $C_{BC} >> C_c$. This is true for the test jig circuit in figure 4.

c. Collector-Base Circuit Inductive

If there is sufficient inductance in series with the by-pass capacitor C_{BC}(lead inductance, for example) the by-pass circuit may be series-resonant at a frequency lower than the measurement frequency. The collector-base loop is then an inductive reactance, and

$$\frac{i_c}{i_e} = \frac{\alpha + j\omega\tau_{bc}(1+j\omega\tau_e)}{(1+j\omega\tau_e)([1-\frac{f}{f_o}^2) + j\omega\tau_{bc}]} \tag{33}$$

resulting in $$\tau = \tau_\alpha + \tau_e - \frac{\tau_{bc}}{h_{fe}} + \tau_{bc}\left[\left(\frac{f_o}{f}\right)^2 - 1\right]^{-1} \tag{34}$$

where $f_o = [2\pi(LC_c)^{1/2}]^{-1}$ is the frequency at which L, the inductance across the collector-base socket pins, and C_c are series resonant.

It is quite likely that the collector-base loop is inductive for most test fixtures of the type exemplified by figure 4. Since equation 34 predicts a large error in τ for test frequencies approaching f_o, it is necessary to determine L so that f_o may be computed.

(1) Determination of Collector-Base Inductance with R-C Networks

The equivalent circuit of the transistor test fixture with an R-C network such as described in Section II 3 in the socket is shown in figure 31. The inductances L_1, L_2, and L_3 are initially unknown.

$$\frac{i_2}{i_1} = \frac{(1 - \omega^2 L_1 C_1)}{(1 + \frac{C_1}{C_2}) - \omega^2 C_1 (L_1 + L_2) + j\omega R_2 C_1} \tag{35}$$

putting i_2/i_1 in the form $A(\omega)e^{-j\theta(\omega)}$ allow one to calculate the absolute magnitude of i_2/i_1 and the phase delay time, $\tau_{ph} = \frac{\theta(\omega)}{\omega}$, in the same manner as outlined in Section IIIa, and these quantities to be compared with vector voltmeter readings. From equation 35,

$$A(\omega) = \left|\frac{i_2}{i_1}\right| = \frac{(1 - \omega^2 L_1 C_1)}{[(1 + \frac{C_1}{C_2}) - \omega^2 C_1 (L_1 + L_2)]^2 + (\omega R_2 C_1)^2} \tag{36}$$

$$\frac{\theta(\omega)}{\omega} = \tau_{ph} = \frac{1}{\omega} \tan^{-1} \frac{\omega R_2 C_1}{[(1 + \frac{C_1}{C_2}) - \omega^2 C_1 (L_1 + L_2)]} \tag{37}$$

Both $A(\omega)$ and $\theta(\omega)$ are independent of the value of L_3. If the correct values of L_1 and L_2 are chosen, the following equalities will be obtained:

$$\left|\frac{i_2}{i_1}\right| \frac{\sqrt{[(1 + \frac{C_1}{C_2}) - \omega^2 C_1 (L_1 + L_2)]^2 + (\omega R_2 C_1)^2}}{(1 - \omega^2 L_1 C_1)} = 1 \tag{38}$$

and

$$\frac{\tan \theta(\omega)}{\omega} [(1 + \frac{C_1}{C_2}) - \omega^2 C_1 (L_1 + L_2)] = R_2 C_1 \tag{39}$$

The degree to which the experimental results fit equations 38 and 39 over the measurement frequency range is a measure of the correctness of the model of the overall vector voltmeter delay time measurement system.

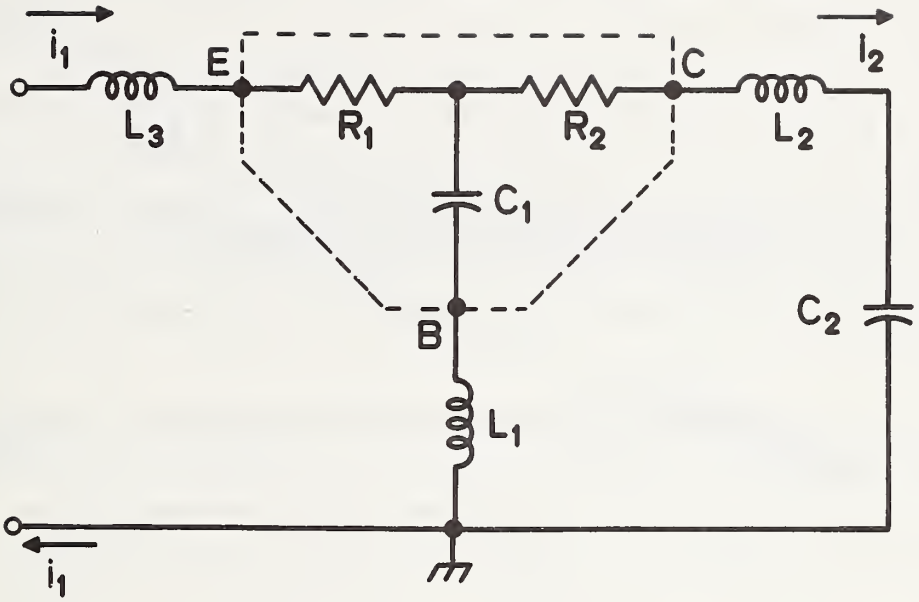

Figure 31. The Equivalent Circuit of the Vector Voltmeter Test Fixture With an R-C Network in the Transistor Socket.

Figure 32 shows measured values of $\tau_{ph} = \frac{\tan \theta(\omega)}{\omega}$, indicated by dotted lines, for the four networks in Table II, compared with computed values of the left-hand side of equation 39, indicated by full lines. In the computation, the value $L_1 + L_2 \equiv L = 45.5$ nH was chosen to minimize the variation with frequency of the left-hand side of equation 39 for network N2, and this same value was then used for the other networks plotted in the figure. The corrected value for each of the four networks is within about 7% of the known R_2C_1 values (see Table II).

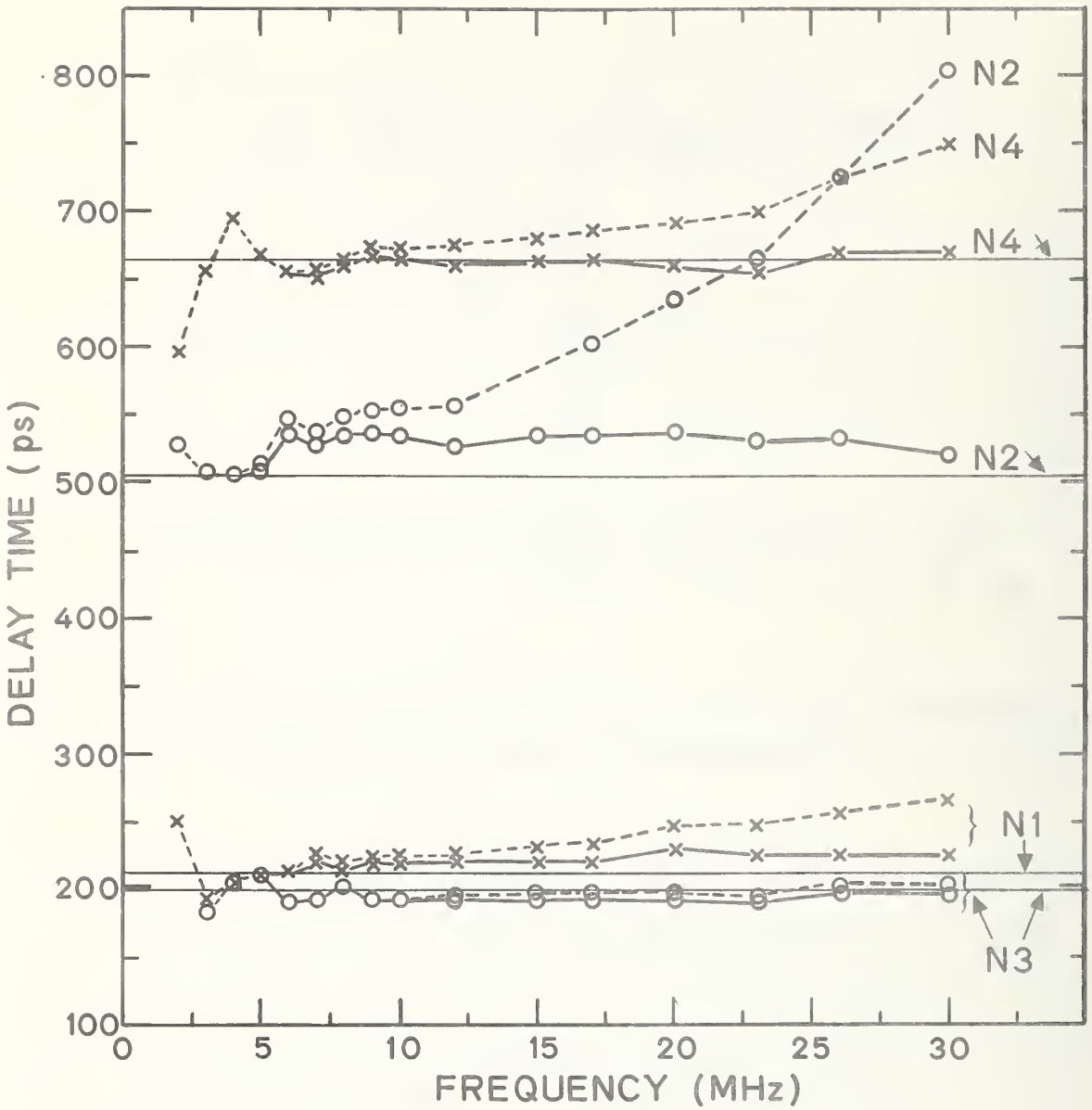

Figure 32. Measured Values of τ_{ph} Indicated by Dotted Lines Compared With Computed Values of the Left-Hand Side of Equation 39 With L = 45.5 nH, for the Four R-C Networks.

The dotted lines in figure 33 show vector voltmeter values of i_2/i_1 for the four networks. Two plots are shown to reduce the tendency of the datum points to obscure one another. The full-line plots are plots of the left-hand side of equation 38 for the four networks with the previously-derived value L = 45.5 nH used, together with the value L_1 = 25.0 nH chosen to minimize the frequency-dependence of the left-hand side of equation 38 for N2. These rssults show that the model postulated in figure 31 is correct in its essential features. Also, since the delay time values read from the vector voltmeter agree within about 7% with those computed, the suitability of the over-all description of the delay-time measurement apparatus is verified.

An estimate of the influence of the parasitic inductance L on transistor measurements can be obtained by assuming that all of it is located in the transistor test fixture and none of it is associated with the R-C networks. If we take as representative the following device parameters r_b = 30 Ω and C_c = 10 pF., then τ_{bc} = 300 ps and f_o = 235 MHz for L = 45.5 nH. The measurement error will be larger the closer the test frequency approaches f_o (see equation 34). At a measurement frequency of 30 MHz, the last term in equation 34 contributes an error of 5 ps, which is approximately the resolution limit of the particular vector voltmeter employed. Thus, for small-signal, high frequency devices (devices with small values of r_b and C_c), the measured delay time is expected to be independent of frequency over the 2 to 30-MHz operating range of the apparatus.

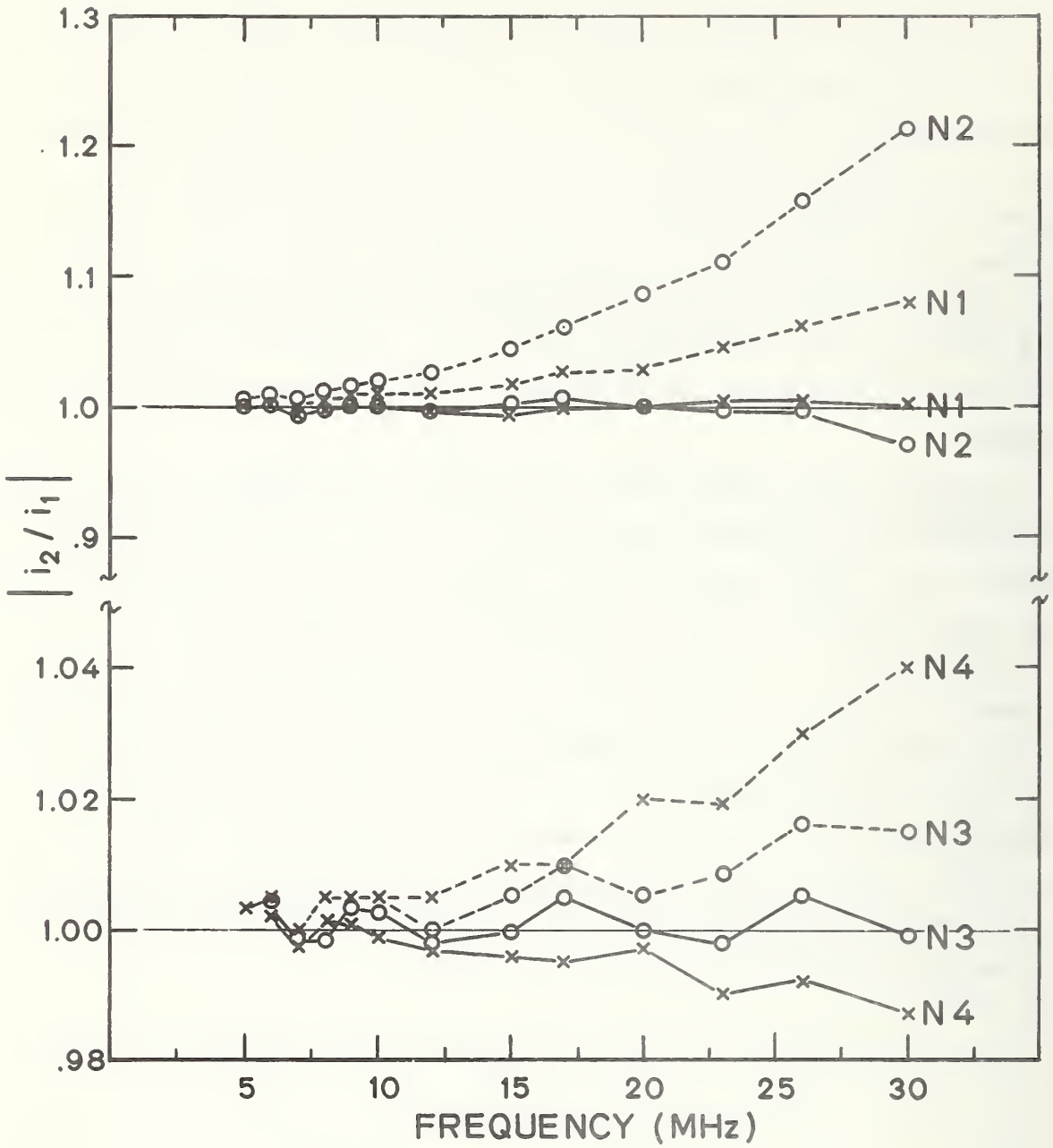

Figure 33. Measured Values of $|i_2/i_1|$ Indicated by Dotted Lines Compared With Computed Values of the Left-Hand Side of Equation 38 With L = 45.5 nH, for the Four R-C Networks.

APPENDIX II

SANDIA BRIDGE DELAY TIME APPARATUS

1. TRANSISTOR ANALYSIS

a. Idealized Measurement Circuit

The bridge equivalent circuit, with the transistor shown by figure 2 in the transistor socket, is shown in figure 34. The following set of equations is solved to determine the bridge balance condition, and hence the relationship between the delay time read and the various transistor time constants for $V_a = V_b = 0$:

$$\frac{i_e \alpha R_z}{1+j\omega\tau_e} - i_{cc} R_z - V_c = 0$$

$$i_e R_z \left(\frac{(1+r_e/R_z) + j\omega\tau_e}{1 + j\omega\tau_e} \right) - i_{cc} \frac{1}{j\omega C_c} = V_e \qquad (40)$$

$$i_e r_b \left(\frac{(1-\alpha) + j\omega\tau_e}{1 + j\omega\tau_e} \right) + i_{cc} \frac{(1+j\omega\tau_{bc})}{j\omega C_c} = 0$$

Equations 40 can be considered as a set in the unknowns i_e, i_{cc}, and V_c, and all of these quantities can be determined simultaneously. For delay time information, however, it is only necessary to solve for V_c. The solution is easily written $V_c = \det V_c / \Delta$ where $\det V_c$ and Δ are the determinants

$$\Delta \equiv \begin{vmatrix} \dfrac{\alpha R_z}{1 + j\omega\tau_e} & -R_z & -1 \\ R_z\left(\dfrac{(1+r_e/R_z) + j\omega\tau_e}{1+ j\omega\tau_e}\right) & \dfrac{-1}{j\omega C_c} & 0 \\ r_b\left(\dfrac{(1-\alpha) + j\omega\tau_e}{1 + j\omega\tau_e}\right) & \dfrac{(1+j\omega\tau_e)}{j\omega C_c} & 0 \end{vmatrix} \quad (41)$$

and

$$\det V_c \equiv \begin{vmatrix} \dfrac{\alpha R_z}{1 + j\omega\tau_e} & -R_z & 0 \\ R_z\left(\dfrac{(1+r_e/R_z) + j\omega\tau_e}{1 + j\omega\tau e}\right) & \dfrac{-1}{j\omega c_c} & V_e \\ r_b\left(\dfrac{(1-\alpha) + j\omega\tau_e}{1 + j\omega\tau_e}\right) & \dfrac{(1 + j\omega\tau_{bc})}{j\omega c_c} & 0 \end{vmatrix} \quad (42)$$

It is readily found that

$$V_c = V_e \frac{[\alpha(1+j\omega\tau_{bc}) + j\omega\tau_{bc}\left((1+j\omega\tau_e) - \alpha\right)]}{(1+j\omega\tau_{bc})\left(r_e/R_z + (1+j\omega\tau_e)\right) + r_b/R_z\left((1+j\omega\tau_e) - \alpha\right)} \quad (43)$$

Equation 43 is exact. We will now make the same (quite generally applicable) assumptions as we did for the vector voltmeter delay time system, i.e., $\omega\tau_e << 1$, $\omega\tau_{bc} << 1$, and $\omega\tau_\alpha << 1$, and we will write $\alpha = \alpha(\omega)e^{-j\omega\tau}\alpha$, and $V_c/V_e = \chi(\omega)e^{-j\omega\tau_t}$, where τ_t is the transistor delay time measured with this system in the absence of extraneous signal pickup. From the description of the bridge balancing procedure, this τ_t is the delay time (as read from the

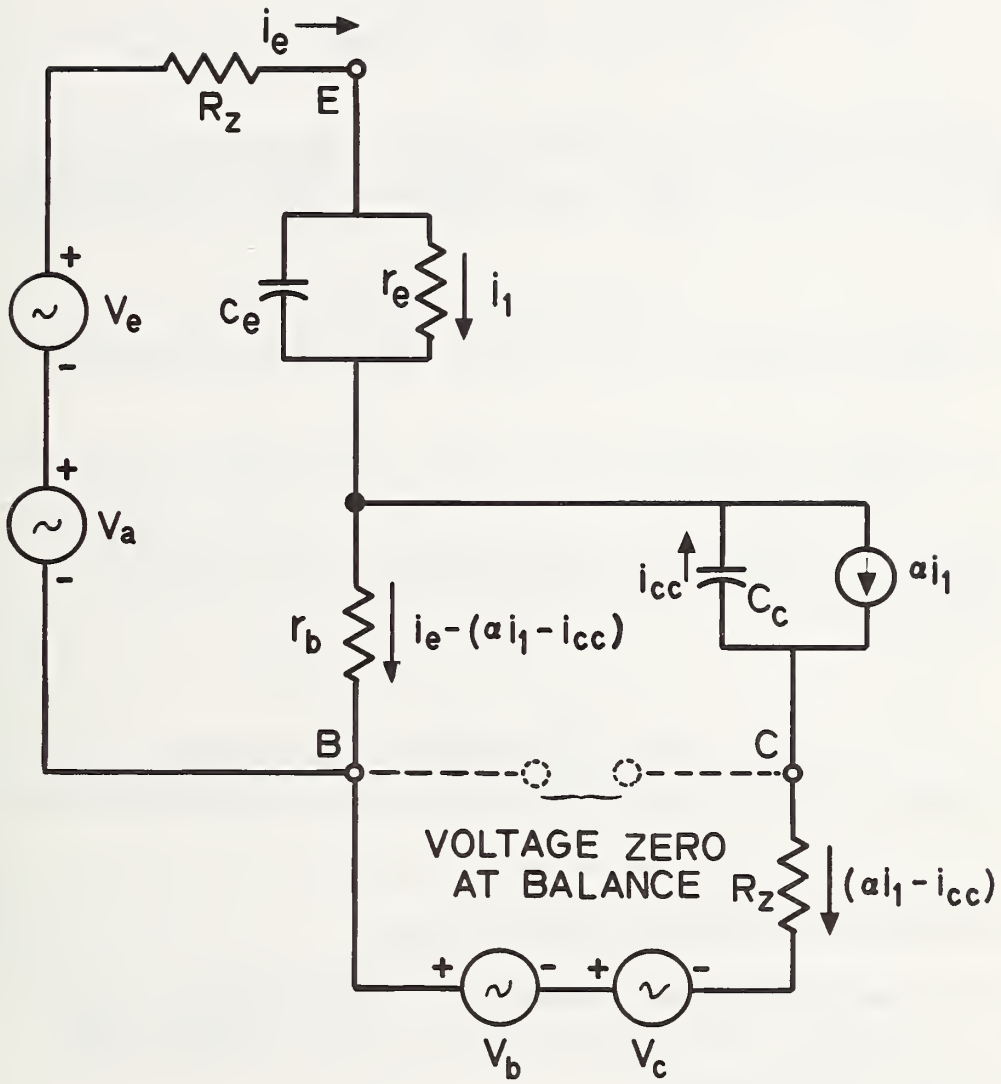

Figure 34. Sandia Bridge Equivalent Circuit With the Transistor Shown by Figure 2 in the Transistor Socket.

calibrated, adjustable delay added to the collector circuit) required to restore the balance condition. For $\omega\tau_t << 1$,

$$\frac{V_c}{V_e} = \left|\chi(\omega)\right| e^{-j\omega\tau_t} = \left|\chi(\omega)\right| (1-j\omega\tau_t)$$

$$= \frac{\alpha(\omega) - j\omega\left[\alpha(\omega)\tau_\alpha - \tau_{bc}\right]}{\left[1 + \frac{r_e+r_b}{R_z}\right] + j\omega\left[\tau_e\left(1 + \frac{r_b}{R_z}\right) + \tau_{bc}\left(1+\frac{r_e}{R_z}\right)\right] - \frac{\alpha(\omega)r_b}{R_z} + j\omega\tau_\alpha\,\alpha(\omega)\,\frac{r_b}{R_z}} \tag{44}$$

Equating imaginary components, it is found with a little manipulation that

$$\tau_t = \frac{1}{1 - \frac{\alpha(\omega)\,r_b}{R_z + r_e + r_b}} \left\{\tau_\alpha + \left(1 - \frac{r_e}{R_z + r_e + r_b}\right)\tau_e - \tau_{bc}/h_{fe}\right\} \tag{45}$$

As for the vector voltmeter analysis (Appendix I), the analysis does not depend on whether or not τ_α and the R-C time constants are frequency-dependent.

b. Correction for Extraneous Signal Pickup

The case of extraneous signal pickup, $V_a \neq 0$ or $V_b \neq 0$, or both, is treated by replacing V_c by $V_c + V_b$ and V_e by $V_e + V_a$ in equation 43. Equation 44, thus, is changed to

$$\frac{V_C}{V_e} = \chi(\omega)\, e^{-j\omega\tau_t} = \chi(\omega)\, e^{-j\omega\tau_t} + \left(\frac{V_a}{V_e}\right)\chi(\omega)\, e^{-j\omega\tau_t} - \left(\frac{V_b}{V_e}\right) \tag{46}$$

where τ_I now represents the indicated delay time which may differ from τ_t, the transistor delay time measured in the absence of V_a and V_b. Equating imaginary components for $Re\ (V_a/V_e) << 1$,

$$\tau_I = \tau_t + \frac{j}{\omega} Im\ (\frac{V_a}{V_e}) - \frac{1}{\chi(\omega)}\ \frac{j}{\omega} Im\ (\frac{V_b}{V_e}) \tag{47}$$

For any practical measurement, $\chi(\omega)$ is found to the required degree of accuracy by taking the real part of the right hand side of equation 44:

$$\chi(\omega) = \frac{\alpha(\omega)\ R_z}{R_z + r_e + r_b\ (1 - \alpha(\omega))} \tag{48}$$

The quantities $\frac{j}{\omega} Im\ (\frac{V_a}{V_e})$ and $\frac{j}{\omega} Im\ (\frac{V_b}{V_e})$ can be determined through the use of known networks in the transistor socket. The simplest network is merely an emitter to collector short circuit. With this in the socket, the bridge equivalent circuit is that shown in figure 35 where the short circuit is represented by the rectangle. At bridge balance,

$$(\frac{V_a}{V_e}) - (\frac{V_b}{V_e}) = [(\frac{V_c}{V_e})_s - 1] \tag{49}$$

With the short circuit replaced by a resistor of value R_s, the condition for bridge balance is

$$(\frac{V_a}{V_e}) - \frac{(R_z + R_s)}{R_z} (\frac{V_b}{V_e}) = [\frac{(R_z + R_s)}{R_z} (\frac{V_c}{V_e})_{rs} - 1] \tag{50}$$

From equations 49 and 50, it is apparent that

$$\left(\frac{V_a}{V_e}\right) = \frac{(R_z + R_s)}{R_s}\left(\frac{V_c}{V_e}\right)_s - \frac{(R_z + R_s)}{R_s}\left(\frac{V_c}{V_e}\right)_{rs} - 1 \qquad (51)$$

and

$$\left(\frac{V_b}{V_e}\right) = \frac{R_z}{R_s}\left(\frac{V_c}{V_e}\right)_s - \frac{(R_z + R_s)}{R_s}\left(\frac{V_c}{V_e}\right)_{rs} \qquad (52)$$

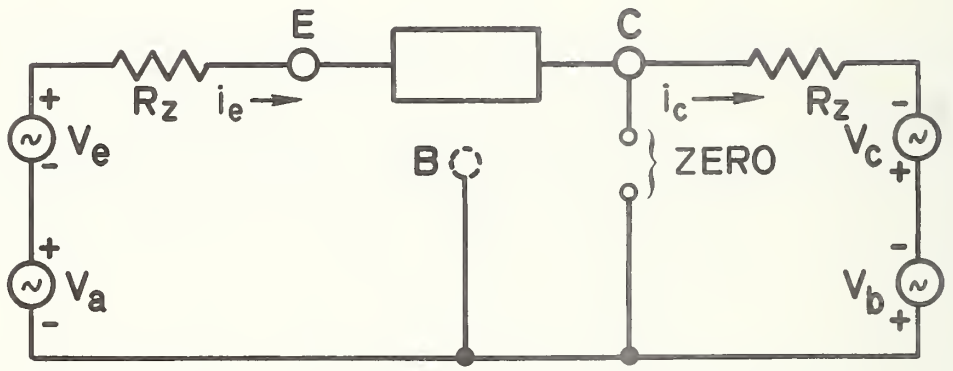

Figure 35. Sandia Bridge Equivalent Circuit Appropriate for a Through Element Such as an Emitter-to-Collector Resistor or Short Circuit, in the Transistor Socket.

The magnitudes of $(V_c/V_e)_s$ and $V_c/V_e)_{rs}$ may be determined to a sufficient degree of accuracy by setting (V_a/V_e) and $V_b/V_e)$ equal to zero in equations 49 and 50.

$$\left| \left(\frac{V_c}{V_e}\right)_s \right| = 1 \tag{53}$$

$$\left| \left(\frac{V_c}{V_e}\right)_{rs} \right| = \frac{R_z}{(R_z + R_s)} \tag{54}$$

Writing $\left(\frac{V_c}{V_e}\right)_s = \left| \left(\frac{V_c}{V_e}\right)_s \right| e^{-j\omega\tau_s}$ and $\left(\frac{V_c}{V_e}\right)_{rs} = \left| \left(\frac{V_c}{V_e}\right)_{rs} \right| e^{-j\omega\tau_{rs}}$ and inserting these and equations 53 and 54 into 51 and 52, taking the imaginary components, it is found that

$$\frac{j}{\omega} Im \left(\frac{V_a}{V_e}\right) = \frac{(R_z + R_s)}{R_s} \tau_s - \frac{R_z}{R_s} \tau_{rs} \tag{55}$$

$$\frac{j}{\omega} Im \left(\frac{V_b}{V_e}\right) = \frac{R_z}{R_s} \tau_s - \frac{R_z}{R_s} \tau_{rs} \tag{56}$$

Finally, inserting equation 48, 55 and 56 into 47, we obtain

$$\tau_m = \tau_I - \tau_s = \tau_t - \left(\frac{1}{h_{fe}} \frac{(R_z + r_b + r_e)}{R_z} + \frac{r_e}{R_z} \right) \frac{j}{\omega} Im \left(\frac{V_b}{V_e}\right) \tag{57}$$

or, by the use of equation 56, τ_m may be written

$$\tau_m = \tau_t - \left(\frac{1}{h_{fe}} \frac{(R_z + r_b + r_e)}{R_s} + \frac{r_e}{R_s} \right) (\tau_s - \tau_{rs}) \tag{58}$$

(1) Test of Correction Technique Using an R-C Netowork

(With an R-C delay time network in the transistor socket, the bridge overall circuit is represented by figure 36.) The set of loop equations is

$$[(R_z + R) - \frac{j}{\omega c} i_e + \frac{j}{\omega c} i_c = (V_e + V_a)]$$

$$R_z i_c - (V_c + V_b) = 0 \tag{59}$$

$$(R_z + R) i_e + (R_z + R) i_c - (V_c + V_b) = (V_e + V_a)$$

with the solution

$$(\frac{V_c}{V_e}) = \frac{R_z}{(R_z+2R)[1+j\omega RC \frac{(R_z+R)}{(R_z+2R)}]} + (\frac{V_a}{V_e}) \frac{R_z}{(R_z+2R)[1+j\omega RC \frac{(R_z+R)}{(R_z+2R)}]} - (\frac{V_b}{V_e}) \tag{60}$$

For $\omega RC << 1$, we have

$$Im\ (\frac{V_c}{V_e}) = -\frac{R_z}{(R_z+2R)} j\omega RC \frac{(R_z+R)}{(R_z+2R)} + \frac{R_z}{(R_z+2R)} Im\ (\frac{V_a}{V_e}) - Im\ (\frac{V_b}{V_e}) \tag{61}$$

The magnitude of (V_c/V_e) can be determined from equation 60 to an accuracy sufficient for our purposes by setting (V_a/V_e) and (V_b/V_e) equal to zero. Writing $(V_c/V_e) = \left|V_c/V_e\right| e^{-j\omega\tau I}$, it is seen that

$$\tau_I = \tau_{RC} \frac{(R_z+R)}{(R_z+2R)} + \frac{j}{\omega} Im\ (\frac{V_a}{V_e}) - \frac{(R_z + 2R)}{R_z} \frac{j}{\omega} Im\ (\frac{V_b}{V_e}) \tag{62}$$

which is equation 13a in section II.

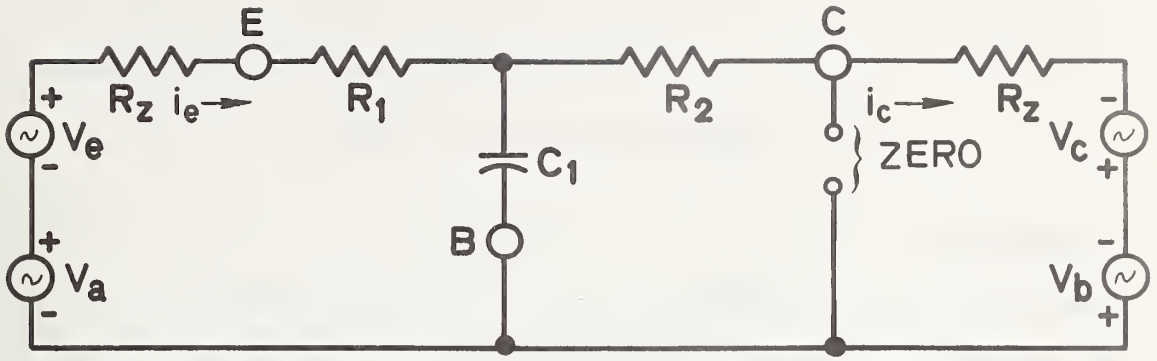

Figure 36. Sandia Bridge Equivalent Circuit for an R-C Network, Such as That Shown in Figure 9, in the Transistor Socket.

With τ_s determined from equations 55 and 56, we may write

$$\tau_m = \tau_I - \tau_s = \tau_{RC} \frac{(R_z+R)}{(R_z+2R)} - \frac{2R}{R_z} \frac{j}{\omega} Im \left(\frac{V_b}{V_e}\right) \tag{63}$$

which is equation 13b in Section II.

By employing equation 56, equation 63 may be written

$$\tau_m = \tau_{RC} \frac{(R_z+R)}{(R_z+2R)} - \frac{2R}{R_s} (\tau_s - \tau_{rs}) \tag{64}$$

which is equation 15a in section II.

APPENDIX III

METHOD FOR EVALUATING PROBES

1. INTRODUCTION

There are two probe configurations, both with three probes in line, but one having the center probe grounded and the other having one end-probe grounded. To simplify evaluation of these probes, the transistor "pads" are considered part of the probe assembly. Thus, stray capacitances and losses resulting from the placement of the pads on the substrate are considered part of the probe. Likewise, contact resistances become part of the probe assembly, and variations in contact resistance appear as variations in the probe parameters. Variations in probe position on the pads may cause a similar variation in the reactive portions of the probe parameters. Thus, the values derived for the elements of the equivalent circuit will be statistically "most likely" values with a statement concerning the likelihood that actual values for a given measurement are within some "acceptable" limits.

The probe assembly, with adapters to miniature coaxial connectors can be represented as shown in figure 37. This configuration can be considered to be two sections of transmission line with a common ground and with some (probably capacitive) coupling, Y_m, between ungrounded conductors. The problem is to evaluate the probe assembly, including adapters, as two two-port networks by measurements at port A and at port B. This can be done if the proper, known impedances are connected at port C and port D.

These known impedances are in six configurations: 1) open-open, 2) resistor-open, 3) short-open, 4) resistor-resistor, 5) short-resistor, and 6) short-short. In every case the resistors are assumed to be pure resistances. Since the resistors are made from very thin metal films and

are very small with very small shunt reactances, they should be frequency independent to frequencies far beyond 2 GHz.

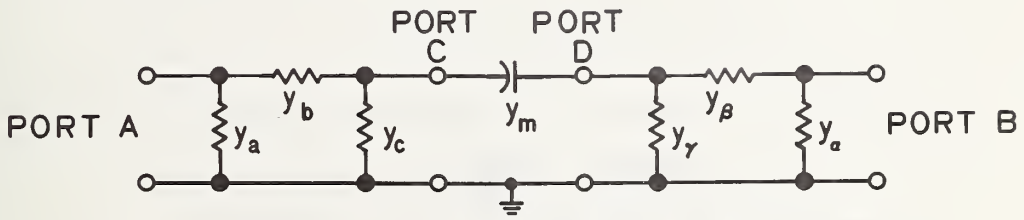

Figure 37. Probe Assembly

Because the pads are considered part of the probe, the open-circuits are perfect opens, unless the processing steps used in depositing resistors and shorts somehow introduce a resistance between pads, but this is unlikely. The capacitance between pads is extremely small, of the order of 2×10^{-15} F, and so the effects of this capacitance will be trivial.

The resistance of the short circuits can be calculated. Assuming 6.35 μm gold for the shorting bar and normal resistivity for gold, the short resistance will be about 2×10^{-3} Ω, which is much less than 50 Ω. The inductance of the short can be calculated and is found to be about 5×10^{-12} H which has a reactance of about 0.032 Ω at 2 GHz. This is about 0.06% of 50 Ω and can be ignored.

2. CENTER PROBE GROUNDED

The grounded-center probe assembly is evaluated as follows:

a. Using the third load configuration (short-open) the probe is as shown in figure 38. From this circuit

$$\text{input at A} = y_1 = y_a + y_b, \text{ and} \tag{65}$$

$$\text{input at B} = y_{11} = y_a + \frac{y_\beta (y_\gamma + y_m)}{y_\beta + y_\gamma + y_m} \tag{66}$$

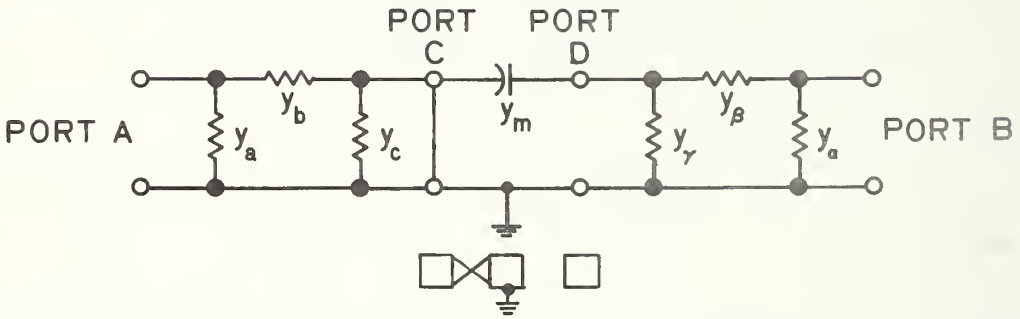

Figure 38. Equivalent Circuit for a Center-Ground Probe Assembly and a Short-open Termination.

Using the same load configuration but reversed, with short at D,

$$\text{input at A} = y_2 = y_a + \frac{y_b (y_c + y_m)}{y_b + y_c + y_m} \tag{67}$$

$$\text{input at B} = y_{12} = y_\alpha + y_\beta \tag{68}$$

b. Using the fifth load configuration (resistor-short) with resistor, y_L, at C, (figure 39) we have

$$\text{input at A} = y_3 = y_a + \frac{y_b\,(y_c + y_L + y_m)}{y_b + y_c + y_L + y_m}, \tag{69}$$

$$\text{input at B} = y_{\alpha} + y_{\beta} \text{ (no new information)}. \tag{70}$$

With the load configuration reversed, with resistor y_L at D,

$$\text{input at A} = y_a + y_b \text{ (no new information)}, \tag{71}$$

$$\text{input at B} = y_{13} = y_{\alpha} + \frac{y_{\beta}\,(y_{\gamma} + y_L + y_m)}{y_{\beta} + y_{\gamma} + y_L + y_m} \tag{72}$$

These two sets of equations (y_1, y_2, y_3 and y_{11}, y_{12}, y_{13}) can be solved for

$$y_{\alpha},\ y_b, \text{ and } y_c + y_m \text{ and}$$

$$y_{\alpha},\ y_{\beta}, \text{ and } y_{\gamma} + y_m$$

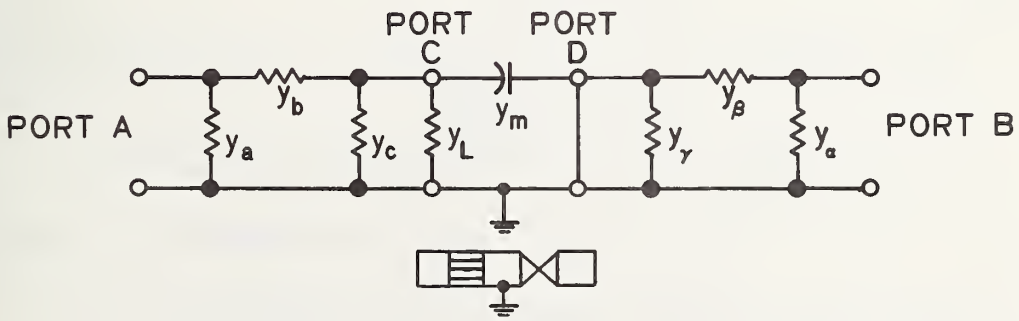

Figure 39. Equivalent Circuit for a Center-Ground Probe Assembly and a Resistor-Short Termination.

These values are not too useful unless y_m can be evaluated or shown to be insignificantly small. To test whether y_m is significant, connect port A to the measuring instrument and with the first standard load configuration (open-open) connected to C and D, connect first a short, then an open to port B. No change in input at port A shows y_m to be insignificant, and it can be dropped from the equations. If y_m is significant, it can be evaluated as follows:

c. With load configuration No. 1 (open-open) connected and port B terminated in an open circuit (quarter-wave short),

$$\text{input at A} = y_3' = y_a + \frac{y_b\left(y_c + \dfrac{y_m\, y_L'}{y_m + y_L'}\right)}{y_b + y_c + \dfrac{y_m\, y_L'}{y_m + y_L'}} \tag{73}$$

$$\text{where } y_L' = y_\gamma + \frac{y_\beta\, y_\alpha}{y_\beta + y_\alpha} \tag{74}$$

Running the program with y_3' instead of y_3 gives values for y_a, y_b, and $y_c + \dfrac{y_m\, y_L'}{y_m + y_L'}$.

y_α and y_β are known, so

$$y_L' = y_\gamma + A, \tag{75}$$

$$\text{where A is } \frac{y_\beta\, y_\alpha}{y_\beta + y_\alpha} \tag{76}$$

Let:

$$\begin{aligned} B &= y_c + y_m && \text{(known)} \\ D &= y_\gamma + y_m && \text{(known)} \\ E &= y_c + \frac{y_m\, y_L'}{y_m + y_L'} && \text{(known)} \end{aligned} \tag{77}$$

$$E = y_c + \frac{y_m (y_\gamma + A)}{y_m + y_\gamma + A} = y_c + \frac{y_m (y_\gamma + A)}{D + A} \tag{78}$$

$$E - B = \frac{y_m (y_\gamma + A)}{D + A} - y_m \tag{79}$$

$$(E - B)(D + A) = y_m (y_\gamma + A) - y_m (D + A) \tag{80}$$

$$= y_m (y_\gamma - D)$$

$$y_m y_\gamma = (E - B)(D + A) + D y_m \tag{81}$$

$$y_\gamma = \frac{(E - B)(D + A)}{y_m} + D \tag{82}$$

$$= y_\gamma + y_m + \frac{(E - B)(D + A)}{y_m}$$

$$y_m^2 = (B - E)(D + A) \tag{83}$$

If each admittance is expressed as a real part, G, and an imaginary part, B,

$$(G_m + j B_m)^2 = [G_B - G_E + j (B_B - B_E)][G_D + G_A + j (B_D + B_A)] \tag{84}$$

$$G_m^2 - B_m^2 + 2j G_m B_m = (G_B - G_E)(G_D + G_A) - (B_B - B_E)(B_D + B_A) \tag{85}$$

$$+ j [(B_B - B_E)(G_D + G_A) + (B_D + B_A)(G_B - B_E)]$$

Equating real and imaginary terms,

$$G_m^2 - B_m^2 = (G_B - G_E)(G_D + G_A) - (B_B - B_E)(B_D + B_A) \equiv K \tag{86}$$

$$2 G_m B_m = (B_B - B_E)(G_D + G_A) + (B_D + B_A)(G_B - G_E) \equiv L \tag{87}$$

If K is positive, use

$$B_m = \frac{L}{2G_m} \tag{88}$$

$$G_m^2 - \frac{L^2}{4G_m^2} = K \tag{89}$$

$$4\,G_m^4 - L^2 = 4\,K\,G_m^2 \tag{90}$$

$$4\,G_m^4 - 4\,K\,G_m^2 - L^2 = 0$$

$$G_m^2 = \frac{4\,K \pm \sqrt{16\,K^2 + 16\,L^2}}{8} \tag{91}$$

$$= \frac{K \pm \sqrt{K^2 + L^2}}{2}$$

G_m is obtained by taking the square root, and

$$B_m = \frac{L}{2G_m} \tag{92}$$

If K is negative, use*

$$G_m = \frac{L}{2B_m} \tag{93}$$

$$\frac{L^2}{4B_m^2} - B_m^2 = K \tag{94}$$

---

* This is done to avoid asking the computer to take the square root of a negative number.

$$L^2 - 4B_m^4 = 4 K B_m^2$$

$$4B_m^4 + K B_m^2 - L^2 = 0$$

$$B_m^2 = \frac{-4 K \pm \sqrt{16 K^2 + 16 L^2}}{}$$

$$= \frac{-K \pm \sqrt{K^2 + L^2}}{2} \qquad (95)$$

B_m is obtained from the square root and

$$G_m = \frac{L}{2B_m}$$

With all parameters known, the probe assembly is completely specified (at one frequency) and the admittance representation can be easily converted to the scattering representation or any other equivalent which may be convenient.

3. END PROBE GROUNDED

The end-grounded probe assembly is evaluated as follows:

a. With standard load configuration No. 3 (short-open) the probe assembly appears as shown in figure 40. From this circuit.

$$\text{input at A} = y_1 = y_a + y_b \qquad (96)$$

$$\text{input at B} = y_{11} = y_\alpha + \frac{y_\beta (y_\gamma + y_m)}{y_\beta + y_\gamma + y_m} \qquad (97)$$

b. Load configuration No. 5. (short-resistor).
From figure 41,

$$\text{input at A} = y_a + y_b \text{ (no new information)}$$

$$\text{input at B} = y_{13} = y_\alpha + \frac{y_\beta (y_\gamma + y_m + y_L)}{y_\beta + y_\gamma + y_m + y_L} \qquad (98)$$

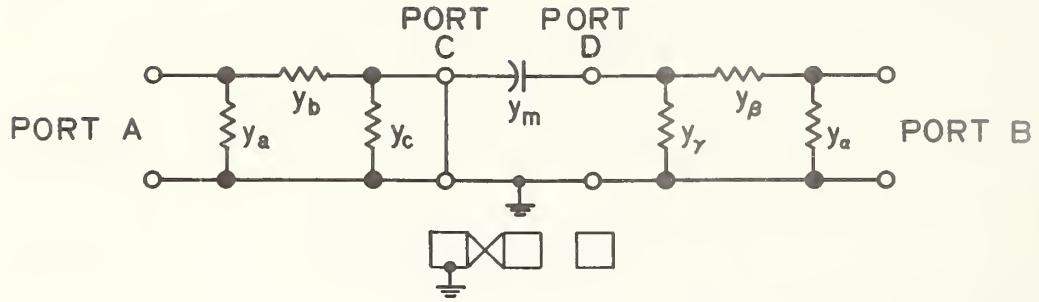

Figure 40. Equivalent Circuit for an End-Ground Probe Assembly and a Short-Open Termination.

c. Load configuration No. 6 (short-short).

From figure 42,

$$\text{input at A} = y_a + y_b \text{ (no new information)},$$
$$\text{input at B} = y_{12} = y_\alpha + y_\beta \text{ } (y_\gamma \text{ is shorted out}). \tag{99}$$

d. Load Configuration No. 3 (short-open) with the addition of a short circuit at port B.

From figure 43,

$$\text{input at A} = y_2 = y_a + \frac{y_b(y_c + y_\gamma + y_\beta)}{y_b + y_c + y_\gamma + y_\beta} \tag{100}$$

Similar expressions can be obtained from port B, but the information is not needed.

e. Load configuration No. 5 (short-resistor) with addition of a short circuit at port B.

From figure 44,

$$\text{input at A} = y_3 = y_a + \frac{y_b\,(y_c + y_L + y_\gamma + y_\beta)}{y_b + y_c + y_L + y_\gamma + y_\beta} \tag{101}$$

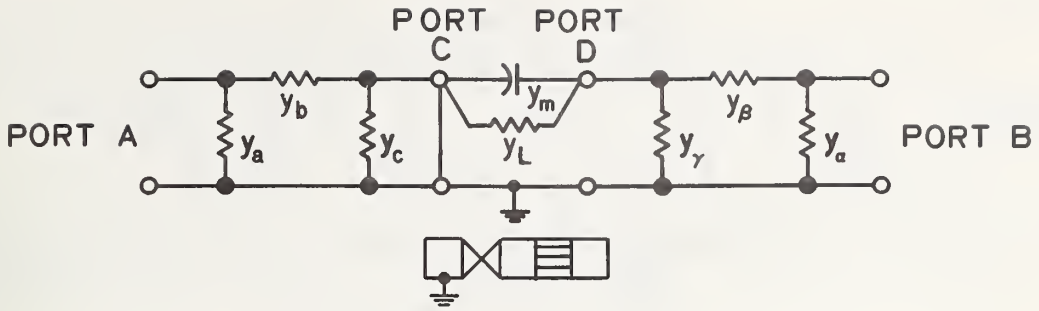

Figure 41. Equivalent Circuit for an End-Ground Probe Assembly and a Short-Resistor Termination.

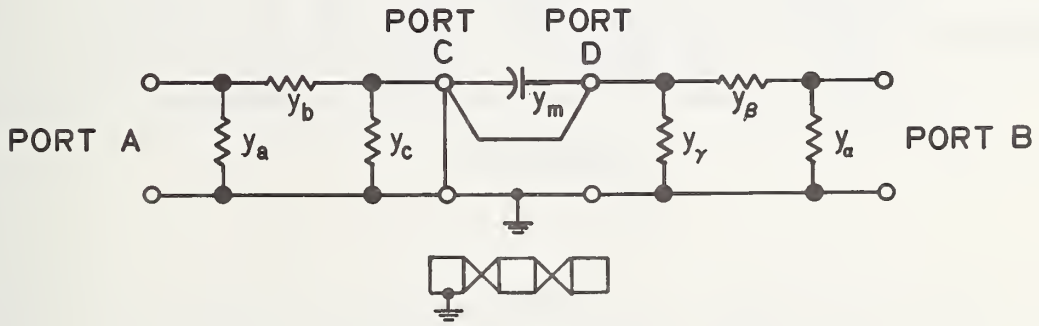

Figure 42. Equivalent Circuit for an End-Ground Assembly and a Short-Short Termination.

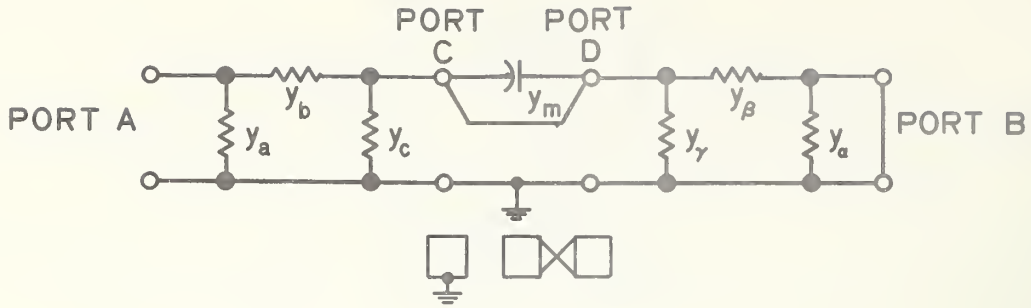

Figure 43. Equivalent Circuit for an End-Ground Probe Assembly and an Open-Short Termination With Port B Short Circuited.

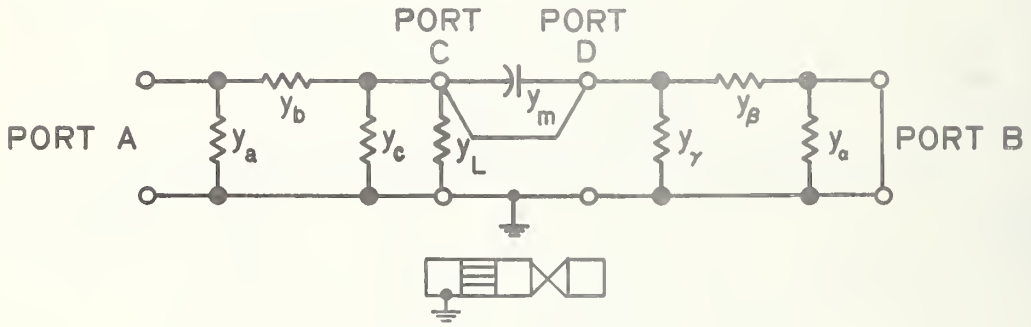

Figure 44. Equivalent Circuit for an End-Ground Probe Assembly and a Resistor-Short Termination With Port B Short Circuited.

No necessary information is needed from port B.
Using y_{11}, y_{12}, and y_{13}, solutions can be obtained for

$$y_\alpha, y_\beta, \text{ and } y_\gamma + y_m$$

Using y_{11}, y_{21}, and y_3, solutions can be obtained for

$$y_a, y_b, \text{ and } y_c + y_\gamma + y_\beta$$

If y_m is insignificant, this is all that is required. If not, load configuration No. 1 (open-open) can be used to give another expression involving y_m, and that quantity can be solved for.

Note that y_L in every case is assumed to be a pure conductance. If this is not so, the program does not apply.

Note that in steps d and e above, a very large y_β will make both y_2 and y_3 degenerate to $y_a + y_b$ exactly as if a short were placed at port C. In this case, use an open on port B (quarter-wave short) and modify the equations accordingly.

APPENDIX IV

CONVERSION OF S-PARAMETERS TO h AND z-PARAMETERS

1. DERIVATION OF h_{21} (h_{fe}) FROM S-PARAMETERS

In a network, figure 26 defined by h parameters, the current-voltage relationships may be written

$$V_1 = h_{11}I_1 + h_{12}V_2,$$
$$I_2 = h_{21}I_1 + h_{22}V_2. \tag{102}$$

The short-circuit forward current transfer ratio is defined as the current developed in the short-circuited output terminals per unit current at the input terminals (reference 15):

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0} \tag{103}$$

In the same network defined by S-parameters, figure 24, the S-parameter description is

$$b_1 = s_{11}a_1 + s_{12}a_2, \tag{104}$$

$$b_2 = s_{21}a_1 + s_{22}a_2, \tag{105}$$

where a_1 and a_2 are waves incident upon the terminals and b_1 and b_2 are waves emerging from them. Z_{01} and Z_{02} are the impedances at the terminals. S_{11} and S_{22} are reflection coefficients, and S_{12} and S_{21} are transmission coefficients; these coefficients are referred to collectively as scattering coefficients.

When the network is terminated in a short circuit, all of the output signal is reflected back to the output terminals, and

$$a_2 = -b_2$$

so that

$$b_2 = s_{21}a_1 + s_{22}(-b_2) \qquad \text{(from 105)}$$

$$= s_{21}a_1 - s_{22}b_2$$

$$b_2 = \frac{s_{21}a_1}{1 + s_{22}} \qquad (106)$$

$$b_1 = s_{11}a_1 + s_{12}(-b_2) \qquad \text{(from 104)}$$

$$= s_{11}a_1 - \frac{s_{12}s_{21}a_1}{1 + s_{22}}$$

$$b_1 = \frac{a_1[s_{11}(1 + s_{22}) - s_{12}s_{21}]}{1 + s_{22}} \qquad (107)$$

The variables in the h-parameter and S-parameter representations are related by the equations (reference 14)

$$V_1 = a_1 + b_1,$$

$$V_2 = a_2 + b_2, \qquad (108)$$

$$I_1 = \frac{a_1 - b_1}{Z_{01}},$$

$$I_2 = \frac{a_2 - b_2}{Z_{02}}$$

The V's and the I's are the rms values of voltage and current, respectively. Both the V's and I's and the a's and b's are usually complex quantities.

If the input and output impedances of the network are equal, $Z_{01} = Z_{02}$, and

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0} = \left.\frac{a_2 - b_2}{a_1 - b_1}\right|_{a_2 = -b_2} = \frac{-2b_2}{a_1 - b_1} \tag{109}$$

Substituting 106 and 107,

$$h_{21} = \frac{\dfrac{-2\, s_{21} a_1}{1 + s_{22}}}{a_1 - \dfrac{a_1 \left[s_{11}(1 + s_{22}) - s_{12}s_{21}\right]}{1 + s_{22}}}$$

$$= \frac{\dfrac{-2\, s_{21}}{1 + s_{22}}}{\dfrac{(1 + s_{22}) - s_{11}(1 + s_{22}) + s_{12}{}^2{}_{21}}{1 + s_{22}}} \tag{110}$$

$$= \frac{-2\, s_{21}}{(1 - s_{11})(1 + s_{22}) + s_{12}s_{21}}$$

2. DERIVATION OF z_{11} FROM S-PARAMETERS

In a network defined by the impedance matrix, the open-circuit input impedance is defined as the ratio of input voltage to input current with the output open circuited,

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2 = 0}$$

Since $I_2 = (a_2 - b_2)/Z_{02}$, the equivalent to setting I_2 to zero in the S-parameter notation is to make a_2 equal to b_2 (figure 24). Equations 104 and 105 can then be rearranged to give

$$b_2 = a_2 = s_{21}a_1 + s_{22}a_2$$

$$a_2 (1 - s_{22}) = s_{21} a_1$$

$$a_2 = \frac{s_{21} a_1}{1 - s_{22}}$$

$$b_1 = s_{11} a_1 + s_{12} a_2$$

$$= s_{11} a_1 + \frac{s_{12}\ 21 a_1}{1 - s_{22}}$$

$$= \frac{s_{11} (1 - s_{22})\ a_1 + s_{12} s_{21} a_1}{1 - s_{22}}$$

$$b_1 = \frac{a_1 [s_{11} (1 - s_{22}) + s_{12} s_{21}]}{1 - s_{22}}$$

$$z_{11} = \frac{V_1}{I_1} = \frac{a_1 + b_1}{\frac{a_1 - b_1}{Z_{01}}}$$

$$\frac{Z_{11}}{Z_{01}} = \frac{a_1 + \frac{a_1 [s_{11} (1 - s_{22}) + s_{12} s_{21}]}{1 - s_{22}}}{a_1 - \frac{a_1 [s_{11} (1 - s_{22}) + s_{12} s_{21}]}{1 - s_{22}}}$$

$$= \frac{(1 - s_{22}) + s_{11} (1 - s_{22}) + s_{12} s_{21}}{(1 - s_{22}) - s_{11} (1 - s_{22}) - s_{12} s_{21}} .$$

$$\frac{Z_{11}}{Z_{01}} = \frac{(1 + s_{11}) (1 - s_{22}) + s_{12} s_{21}}{(1 - s_{11}) (1 - s_{22}) - s_{12} s_{21}} . \qquad (111)$$

Note that in equation 111, Z_{11} is normalized to the impedance at the input terminals of the network.

Equations relating the y parameters or the other h and z-parameters to the S-parameters can be derived in a similar fashion.

APPENDIX V

PLAN FOR AN INTERLABORATORY COMPARISON OF TRANSISTOR SCATTERING PARAMETER MEASUREMENTS

1. PURPOSE

The purpose of the interlaboratory comparison is to assess the variability of the S-parameter measurement systems as used by the participants.

The method employed is to measure selected transistors on each of the S-parameter measurement systems and to compare the results obtained. As a check against possible changes in the transistor parameters and variability introduced by auxiliary systems such as transistor fixtures and bias supplies, a coaxial attenuator and passive networks will be included in the measurements. For each device, both magnitude and phase of S_{11}, S_{21}, S_{12}, and S_{22} will be measured as a function of frequency. Each of the passive elements will be measured more than once on each system to obtain a measure of the variability of the individual systems.

2. CONDITIONS BEING STUDIED

The test plan is designed to determine the following:

a. Differences in the results obtained from the S-parameter test sets when measuring the same device, including effects of the operator and the associated fixtures and bias supply systems.

b. Differences introduced by transistor fixtures.

c. The effect of transistor bias on the measurements. The measurements are relatively insensitive to changes in V_{CE}, but are very sensitive to changes in emitter current, especially at the lower values of emitter current. Five percent accuracy in the measurement of V_{CE} and 1 % accuracy in the measurement of emitter current would be desirable. These accuracies are not

specified for the round robin, however, because the intent is to measure the transistors by the procedure normally used by the participants. Measurement of the passive networks will provide a measure of the variability of the S-parameter measurement systems which is independent of bias levels. The tests may disclose that more accurate control of bias levels is required for repeatable transistor measurements.

3. CONDITIONS NOT BEING STUDIED

The transistors themselves are not under study. NBS will record the characteristics of each transistor before the testing begins and will periodically check transistor performance against these characteristics during the round robin to detect any changes that may occur.

While transistor case temperature may affect the data, it is low enough to make special provisions for the control of transistor case temperature unnecessary at the power levels used in these tests provided the laboratory temperature is within the range 68 to 77°F (20 to 25°C).

4. DEVICES TO BE TESTED

The following devices will be circulated for test to each of the participants (all participants will test the same devices):

a. Two coaxial attenuators with a length of semi-rigid coax for connecting them in series to the test set.

b. A transistor fixture to adapt the S-parameter test set for the measurement of transistors in TO-18 and TO-72 packages.

c. Three R-C networks mounted on transistor TO-72 headers.

d. Six transistors of each of the following types: 2N709, 2N918, and 2N3960.

5. TEST EQUIPMENT

Each participant shall furnish the following information about the characteristics of his measurement system:

a. The manufacturer, model number and serial number of the equipment used in making the measurements.

b. The method of reducing the RF drive to the transistor under test if one is used.

c. The method of setting the transistor bias levels and their accuracy. Indicate how the accuracy is verified.

6. MEASUREMENTS

The transistors to be tested have been divided into A and B groups, each group comprising three transistors of each type. These are to be tested along with the passive elements as follows:

a. Record the laboratory ambient temperature.

b. Calibrate the S-parameter measurement system without the transistor fixture at frequencies between 200 MHz and 2 GHz in increments of 100 MHz and record the procedure used. Use the coaxial link furnished by NBS as the through line, connecting it so that the terminal marked A is connected to the A port of the S-parameter test set and the terminal marked B is connected to the B port. The electrical length of this link is 46.525 cm. After calibration, change the transmission linearization to 46.525 cm.

c. Connect the 10-dB attenuators to the output ports of the test set, with the end marked A connected to the A port and the end marked B to the B port. Connect the attenuators in series by means of the coaxial link, again connecting it so that the terminal marked A connects to the attenuator connected to the A port and the terminal marked B connects to the attenuator connected to the B port. Measure and record the S-parameters at frequencies between 200 MHz and 2 GHz in 100-MHz increments.

d. Using the calibration standards (THRU LINE and SHORT) provided by NBS where applicable, calibrate the S-parameter measurement system with the NBS transistor fixture connected to the output ports at frequencies between 200 MHz and 2 GHz in 100-MHz increments, and record the procedure used.

e. Measure and record the S-parameters of the R-C networks at frequencies between 200 MHz and 2 GHz in 100-MHz increments using the common-base configuration on the NBS transistor fixture.

f. Connect the participant's transistor fixture to the output ports of the S-parameter system and calibrate the system using the participant's calibration standards at frequencies between 200 MHz and 2 GHz in 100-MHz increments.

g. Connect each of the devices in turn to the participant's transistor fixture and measure and record the S parameters of the device.

(1) Measure the R-C networks in the common-base configuration at frequencies between 200 MHz and 2 GHz in 100-MHz increments.

(2) Measure the transistors of Group A in the common-emitter configuration under the bias conditions and at the frequencies listed in Table VI.

Table VI

Bias and Measurement Conditions Used for Three Transistor Types

Type	V_{CE} (Volts)	I_E (ma)	FREQUENCY-(MHz) START	STOP	INCREMENT
2N709	5	1.6, 2.0, 2.5, 4.0, 5.0, 8.0, 10.0	200	1000	100
2N918	5	1.6, 2.0, 2.5, 4.0, 5.0, 8.0, 10.0	200	1000	100
2N3960	5	1.6, 2.0, 2.5, 4.0, 5.0, 8.0, 10.0	200	1800	100

(3) Repeat the measurements on the R-C networks in the common-base configuration at frequencies between 200 MHz and 1800 MHz in 100-MHz increments.

(h) Recalibrate the system with the NBS transistor fixture connected to the output ports (using the same calibration procedure as in d) and remeasure and record the S-parameters of the R-C networks in the common-base configuration at frequencies between 200 MHz and 2 GHz in increments of 100 MHz.

i. Recalibrate the system without the transistor fixture (using the same calibration procedure as in b) and remeasure and record the S-parameters of the 10-dB attenuators connected in series at frequencies between 200 MHz and 2 GHz in 100-MHz increments.

j. Record the laboratory ambient temperature.

k. On a different day, repeat the measurement outlined in a thru j but use the transistors of Group B in step g (2).

7. DATA TO BE FURNISHED TO NBS

The following information is the minimum required:

a. The manufacturer, model number and serial number of the equipment used for the measurements.

b. The step-by-step procedure used in calibrating the S-parameter measurement system. If the manufacturer's procedure is followed, a statement to this effect with a reference to the document (including date or edition) and page where the procedure is found is sufficient. Be sure to record any deviations from the stated procedure.

c. The step-by-step procedure used in calibrating the system when the transistor fixture is added. If the manufacturer's procedure is followed, a statement to this effect with a reference to the document (including date or edition) and page where the procedure is found is sufficient. Be sure to record any deviations from the stated procedure.

d. The method of reducing the RF drive to the transistor under test if one is used.

e. The method of setting the bias levels, the accuracy of these levels, and the method of verifying the accuracy.

f. A tabulation of S-parameters versus frequency for each of the devices tested. To reduce the time required for processing the data at NBS and to minimize errors, we would prefer to receive the data punched on paper tape if this is possible; if this would entail extra work on the part of the participants, a data printout is acceptable. Each set of data should

be identified with the name of the device tested (if a transistor include both the type number and the letter identifying the sample), and the conditions of test. This information should be written on the tape ahead of the data. Leave a gap of 3 or 4 inches on the tape between sets of data.

The beginning of each tape must be visibly marked to identify the participant and the contents of the tape. This can be done by marking the tape with the identity of the participant and listing the contents of the tape, for example, NBS, passive devices, first set, first day; NBS, Group A, 2N709; etc. An alternate method would be to mark the tape with the identity of the participant and an identifying letter or number and provide the legend on a separate sheet.

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15. SUPPLEMENTARY NOTES

16. ABSTRACT (*A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.*)

Two instruments for transistor delay-time measurements, the vector voltmeter and Sandia bridge, were analyzed and comparative measurements were made on several types of commercial and two special transistors. It was found that extraneous pickup at the measurement frequency can cause large errors in measured delay time. A technique for minimizing these errors was developed and verified for the Sandia bridge by removing the frequency dependence of delay force, probe tip protrusion and lateral motion (skating) with loading were recorded for special probe assemblies to be used in an automatic wafer prober for measurements on transistors in custom-designed integrated circuit wafers. The data is used to assist in adjusting the probers. A technique was developed for determining the effects of the probe assemblies on transistor measurements made from 0.1 to 2.0 GHz. Each probe assembly may be represented by an equivalent circuit consisting of three unknowns; these unknowns are determined by making impedance measurements at the input connectors with the probe tips contacted by combinations of open circuits, short circuits, and resistors of known value. Arrays of such terminations were successfully fabricated and characterized. An S-parameter interlaboratory testing program was developed. The plan calls for six of each of three types of transistors to be measured by participants at frequencies from 0.11 to 2.0 GHz. Additionally, a 10-dB attenuator and R-C networks on TO-72 headers are to be circulated to pinpoint measurement discrepancies.

17. KEY WORDS (*six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons*)

Delay time; electronics; high-frequency probes; Sandia bridge; scattering; S-parameters; vector voltmeter; transistors.

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